Exhibit 2

~~IN THE~~ UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., Plaintiff, ~~v.~~ vs. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., Defendants.	~~Civil Action~~Case No. 2:22-cv-~~00293~~ 293-JRG JURY TRIAL DEMANDED **LEAD CASE**
NETLIST, INC., **Plaintiff,** **vs.** **MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; MICRON TECHNOLOGY TEXAS LLC,** **Defendants.**	**Case No. 2:22-cv-294-JRG** **JURY TRIAL DEMANDED**

~~FIRST~~SECOND AMENDED COMPLAINT AGAINST SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., AND SAMSUNG SEMICONDUCTOR, INC.

1. ~~1.~~Plaintiff Netlist, Inc. ("Netlist"), by its undersigned counsel, for its ~~First~~Second Amended Complaint against defendants Samsung Electronics Co., Ltd.

("SEC"), Samsung Electronics America, Inc. ("SEA"), and Samsung Semiconductor, Inc. ("SSI") (collectively, "Samsung" or "Defendants"), states as follows, with knowledge as to its own acts, and on information and belief as to the acts of others:

2. ~~2.~~This action involves Netlist's U.S. Patent Nos. 7,619,912 (the "'912 patent," Exhibit 1), 11,093,417 (the "'417 patent," Exhibit 2), ~~and~~ 9,858,215 (the "'215 patent," Exhibit 3), and **10,268,608 (the "'608 patent")** (the "Patents-in-Suit").

I. THE PARTIES

3. ~~3.~~Plaintiff Netlist is a corporation organized and existing under the laws of the State of Delaware, having a principal place of business at 111 Academy Drive, Suite 100, Irvine, CA 92617.

4. ~~4.~~On information and belief, SEC is a corporation organized and existing under the laws of the Republic of Korea, with its principal place of business at 129 Samsung-ro, Yeongtong- gu, Suwon, Gyeonggi, 16677, Republic of Korea. On information and belief, SEC is the worldwide parent corporation for SEA and SSI, and is responsible for the infringing activities identified in this ~~First~~**Second** Amended Complaint. On information and belief, SEC's Device Solutions division is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. On information and belief, SEC is also involved in the design, manufacture, and provision of products sold by SEA.

5. ~~5.~~On information and belief, SEA is a corporation organized and existing under the laws of the State of New York. On information and belief, SEA, collectively with SEC, operates the Device Solutions division, which is involved in the design,

manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. Defendant SEA maintains facilities at 6625 Excellence Way, Plano, Texas 75023. SEA may be served with process through its registered agent for service in Texas: CT Corporation System, 1999 Bryan Street, Suite 900, Dallas, Texas 75201-3136. SEA is a wholly owned subsidiary of SEC.

6. ~~6.~~On information and belief, SSI is a corporation organized and existing under the laws of the State of California. On information and belief, SSI, collectively with SEC, operates the Device Solutions division, which is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. On information and belief, Defendant SSI maintains facilities at 6625 Excellence Way, Plano, Texas 75023. Defendant SSI may be served with process through its registered agent National Registered Agents, Inc., 1999 Bryan St., Ste. 900, Dallas, TX 75201-3136. On information and belief, SSI is a wholly owned subsidiary of SEA.

7. ~~7.~~On information and belief, Defendants have used, sold, or offered to sell products and services, including the Accused Instrumentalities, in this judicial district.

II. JURISDICTION AND VENUE

8. ~~8.~~Subject matter jurisdiction is based on 28 U.S.C. § 1338, in that this action arises under federal statute, the patent laws of the United States. 35 U.S.C. §§ 1, *et seq*.

9. ~~9.~~Each Defendant is subject to this Court's personal jurisdiction consistent with the principles of due process and the Texas Long Arm Statute. Tex. Civ. Prac. & Rem. Code §§ 17.041, *et seq*.

10. ~~10.~~Personal jurisdiction exists over the Defendants because each Defendant has sufficient minimum contacts and/or has engaged in continuous and systematic activities in the forum as a result of business conducted within the State of Texas and the Eastern District of Texas. Personal jurisdiction also exists over each Defendant because each, directly or through subsidiaries, makes, uses, sells, offers for sale, imports, advertises, makes available, and/or markets products within the State of Texas and the Eastern District of Texas that infringe one or more claims of the Patents-in-Suit. Further, on information and belief, Defendants have placed or contributed to placing infringing products into the stream of commerce knowing or understanding that such products would be sold and used in the United States, including in this District.

11. ~~11.~~Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b) and (c) and/or 1400(b). For example, SEC maintains a regular and established place of business in this judicial district at 6625 Excellence Way, Plano, Texas 75023, and has committed acts of infringement in this judicial district. As another example, SEA maintains a regular and established place of business in this judicial district at 6625 Excellence Way, Plano, Texas 75023, and has committed acts of infringement in this judicial district. Venue is also proper for SSI because it maintains a regular and established place of business in this judicial district at 6625 Excellence Way, Plano, Texas 75023, and has committed acts of infringement in this judicial district.

12. ~~12.~~Defendants have not contested proper venue in this District. *See, e.g.*, Answer at ¶ 12, *Emergent Mobile LLC v. Samsung Elecs. Co., Ltd.*, No. 2:22-cv-107, Dkt. 12 (E.D. Tex. Aug. 3, 2022); Answer at ¶ 10, *Arbor Global Strategies LLC v. Samsung*

Elecs. Co., Ltd., No. 2:19-cv- 333, Dkt. 43 (E.D. Tex. Apr. 27, 2020); Answer at ¶ 29, *Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.*, No. 2:19-cv-347, Dkt. 14 (E.D. Tex. Feb. 12, 2020).

III. FACTUAL ALLEGATIONS

Background

13. ~~13.~~Since its founding in 2000, Netlist has been a leading innovator in high-performance memory module technologies. Netlist designs and manufactures a wide variety of high-performance products for the cloud computing, virtualization and high-performance computing markets. Netlist's technology enables users to derive useful information from vast amounts of data in a shorter period of time. These capabilities will become increasingly valuable as the volume of data continues to dramatically increase.

14. ~~14.~~The technologies disclosed and claimed in the Patents-in-Suit relate generally to memory modules. In many commercial products, a memory module is a printed circuit board that contains, among other components, a plurality of individual memory devices (such as DRAMs). The memory devices are typically arranged in "ranks," which are accessible by a processor or memory controller of the host system. A memory module is typically installed into a memory slot on a computer motherboard and serve as memory for computer systems.

15. ~~15.~~Memory modules are designed for various purposes, including use in server computers supporting cloud-based computing and other data-intensive applications. The structure, function, and operation of memory modules are often defined, specified, and standardized by the JEDEC Solid State Technology Association ("JEDEC"), a standard-

setting body for the microelectronics industry. Memory modules are typically characterized by the generation of DRAM on the module (*e.g.*, DDR4, DDR3) and the type of module (*e.g.*, RDIMM, LRDIMM).

16. ~~16.~~Dual in-line memory modules ("DIMMs") are a type of memory module which generally includes SDRAMs mounted in a printed circuit board with other components, *e.g.*, serial presence detect ("SPD") and Hub with thermal sensors.

17. ~~17.~~The load-reduced dual in-line memory modules ("LRDIMMs") and registered DIMMs ("RDIMMs") are types of memory modules that generally include SDRAMs mounted on a printed circuit board. RDIMMs and LRDIMMs typically also include an RCD for transmitting control and address signals to the SDRAMs, and LRDIMMs typically also include data buffers between the host controller and memory devices.

18. ~~18.~~Netlist designs and manufactures a wide variety of high-performance products for the cloud computing, virtualization, and high-performance computing markets. Netlist's technology enables users to derive useful information from vast amounts of data in a shorter period of time. These capabilities will become increasingly valuable as the volume of data continues to dramatically increase.

19. ~~19.~~Netlist has a long history of being the first to market with disruptive new products such as the first LRDIMM, HyperCloud®, based on Netlist's distributed buffer architecture. Netlist's—and the industry's—first LRDIMM product demonstrated what was previously thought to be impossible: that a server could be fully loaded with memory and still operate at the highest system speeds available at the time. Netlist's

innovative products built on Netlist's early pioneering work in areas such as embedding passives into printed circuit boards to free up board real estate, doubling densities via quad-rank double data rate (DDR) technology, and other off- chip technology advances that result in improved performance and lower costs compared to conventional memory.

The Asserted '912 Patent

20. ~~20.~~The '912 patent is entitled "Memory Module Decoder." Netlist owns the '912 patent by assignment from the listed inventors Jayesh R. Bhakta and Jeffrey C. Solomon. The '912 patent was filed as Application No. 11/862,931 on September 27, 2007, issued as a patent on November 17, 2009, and claims priority to three provisional applications: Nos. 60/588,244 filed on July 15, 2004 60/550,668 filed on March 5, 2004, and 60/575,595 filed on May 28, 2004. The '912 patent also claims priority to application, filed July 1, 2005, now U.S. Patent No. 7,289,386, which is a continuation-in-part of application No. 11/075,395, filed March 7, 2005, now U.S. Patent No. 7,286,436.

21. ~~21.~~Samsung had knowledge of the '912 patent no later than July 6, 2021, when it received a request for indemnification from Google LLC ("Google") in connection with Netlist's assertion of the '912 patent against Google in *Netlist, Inc. v. Google LLC*, No. 3:09-cv-05718 (N.D. Cal.). *Samsung Elec. Co. Ltd. et. al. v. Netlist, Inc.*, No. 21-cv-1453-RGA, Dkt. 14, ¶ 43 (D. Del. Jan. 18, 2022).

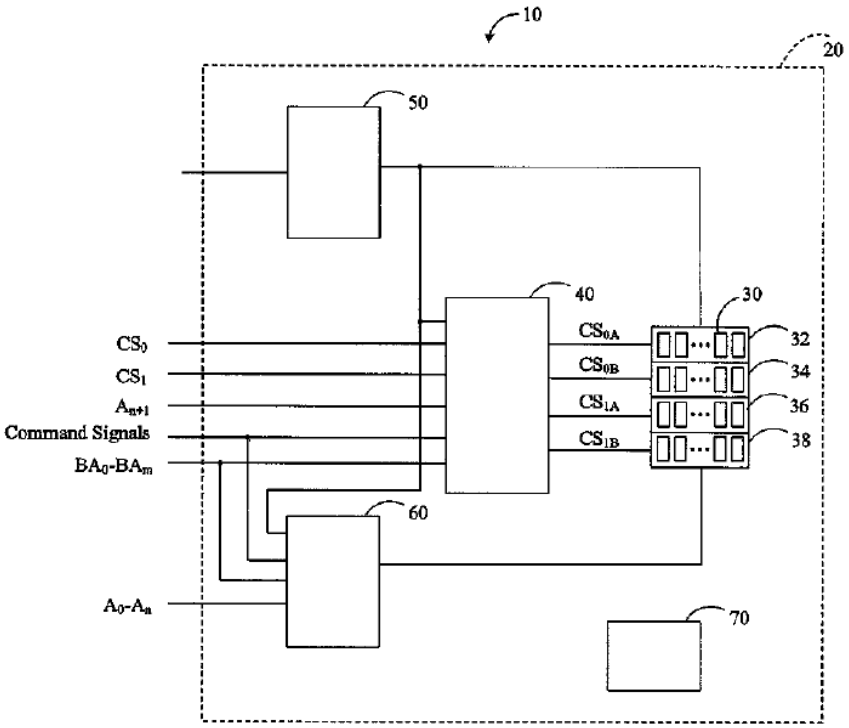
22. ~~22.~~The '912 patent relates to memory module technology, and more specifically, to a concept called rank multiplication. A memory module is a device that contains individual memory devices arranged in "ranks" on a printed circuit board. At the

time of the invention, most computer systems supported accessing only one or two ranks, limiting the number of ranks that can be added per memory module. Exhibit 1, 1:20-2:42.

23. ~~23.~~The '912 patent teaches that one way to upgrade the memory capacity of a memory module is to use on-module logic to present a memory module with, *e.g.*, 2n physical ranks of memory devices, as a module with n (virtual) ranks to the computer system. *Id.*, 6:64-7:19. In this way, "even though the memory module 10 actually has the first number of [physical] ranks of memory devices 30, the memory module 10 simulates a virtual memory module by operating as having the second number of [logical or virtual] ranks of memory devices 30." *Id.*, 7:9-13. This technique is commonly referred to as "rank multiplication."

24. ~~24.~~Rank multiplication allows a designer to expand the number of ranks and hence the total memory capacity on a memory module. It also enables them to construct a memory module of a given capacity using lower density memory devices that often cost less. *Id.*, 4:42-58, 22:5-14. For example, for the same 1 GB memory capacity, it could be more cost-effective to use thirty-six 256-Mb DRAMs arranged in 4 ranks than eighteen 512-Mb DRAMs arranged in two ranks. *Id.*, 4:42-58, 4:59-5:5.

25. ~~25.~~Figure 1A illustrates an example of a memory module with rank multiplication capability. The memory module has a register 60 and a logic element 40.



26. ~~26.~~The logic element receives a set of input control signals from the computer system that include chip-select signals CS_0-CS_1, address signal A_{n+1}, and bank address signals BA_0-BA_m. *Id.*, 7:35-53; Fig. 1A. From the computer system's perspective, it is connected to only two ranks of memory devices, to be selected by CS_0 or CS_1, even though the memory devices are arranged in four physical ranks. *Id.*, 6:55-7:19. In response to the received input control signals, the logic element on the memory module generates a set of output control signals, corresponding to the four physical ranks of the memory devices. *Id.*, 6:61-63. The logic element 40 also receives command signals (such as read/write) from the computer system. *Id.*, 6:55-61, 7:46-53. In response to the command signal and the input signals, the logic element transmits the command signal to the memory

devices on the selected rank of the memory module. *Id.* In some embodiments, command signals are transmitted to only a single memory device on a multi-device rank at a time.

27. ~~27.~~In 2009, Netlist served a complaint alleging infringement of the '912 patent on Google and Inphi in separate proceedings in the Northern District and Central District of California, respectively. In 2010, Google, Inphi, and a third entity—Smart Modular Technologies ("SM")—sought *inter partes* reexamination of the '912 patent. SM was not accused of infringement by Netlist; but it is a long-time memory development partner with Samsung. The PTO ordered reexamination and merged the three proceedings. The consolidated proceeding examined every single claim of the '912 patent, including claim 16. Over the course of the reexamination, the Patent Trial and Appeal Board twice affirmed the validity of claim 16, and the Federal Circuit summarily affirmed the Board.

The Asserted '417 Patent

28. ~~28.~~The '417 patent is entitled "Memory Module With Data Buffering." Netlist owns the '417 patent by assignment from the listed inventors Jayesh R. Bhakta and Jeffrey C. Solomon. The '417 patent was filed as Application No. 16/695,020 on November 25, 2019, issued as a patent on August 17, 2021, and claims priority to five provisional applications: Nos. 60/645,087, filed on January 19, 2005, 60/590,038, filed on July 21, 2004, 60/588,244 filed on July 15, 2004, 60/550,668 filed on March 5, 2004, and 60/575,595 filed on May 28, 2004.

29. ~~29.~~Samsung had knowledge of the '417 patent via notice of U.S. Patent Application No. 16/695,020 on August 2, 2021 through Samsung's access to Netlist's

patent portfolio docket. Samsung has also gained knowledge of the '417 patent via this ~~First~~Second Amended Complaint.

30. ~~30.~~The '417 patent relates to a memory module operable to communicate data with a memory controller via a N-bit wide memory bus, where the memory module includes memory devices arranged in a plurality of N-bit wide ranks, with logic that is configurable to receive a set of input address and control signals associated with a read or write memory command and output registered address and control signals and data buffer control signals. As summarized in the Abstract, the memory module further includes circuitry coupled between the memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, where the circuitry is configurable to "enable registered transfers of N-bit wide data signals associated with the memory read or write command between the N-bit wide memory bus and the memory devices in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module, which is greater than an actual operational CAS latency of the memory devices."

The Asserted '215 Patent

31. ~~31.~~The '215 patent is entitled "Memory Module With Data Buffering." Netlist owns the '215 patent by assignment from the listed inventors Jayesh R. Bhakta and Jeffrey C. Solomon. The '215 patent was filed as Application No. 14/715,486 on May 18, 2015, issued as a patent on January 2, 2018, and claims priority to five provisional applications: Nos. 60/645,087, filed on January 19, 2005, 60/590,038, filed on July 21, 2004, 60/588,244 filed on July 15, 2004, 60/550,668 filed on March 5, 2004, and 60/575,595 filed on May 28, 2004.

32. ~~32.~~Samsung had knowledge of the '215 patent no later than August 2, 2021 via its access to Netlist's patent portfolio docket. Samsung has also gained knowledge of the '215 patent via this ~~First~~**Second** Amended Complaint.

33. ~~33.~~The '215 patent relates to a memory module that is operable to communicate data with a memory controller via a memory bus in response to memory commands received from the memory controller. The memory module includes a plurality of memory integrated circuits arranged in ranks, at least one first memory integrated circuit in a first rank and at least one second memory integrated circuit in a second rank, and a buffer coupled between the at least one first memory integrated circuit and the memory bus and between the at least one second memory integrated circuit and the memory bus. As summarized in the Abstract, the "memory module further comprises logic providing first control signals to the buffer to enable communication of a first data burst between the memory controller and the at least one first memory integrated circuit through the buffer in response to a first memory command, and providing second control signals to the buffer to enable communication of a second data burst between the at least one second memory integrated circuit and the memory bus through the buffer in response to a second memory command."

The Asserted '608 Patent

34. The '608 Patent is entitled "Memory Module With Timing-Controlled Data Paths in Distributed Data Buffers." Netlist owns the '608 Patent by assignment from the listed inventors Hyun Lee and Jayesh R. Bhakta. The '608 Patent was filed as Application No. 15/820,076 on November 21, 2017, issued as a patent on April 23,

2019, and claims priority to, among others, a utility application filed on July 27, 2013 (No. 13/952,599) and a provisional application filed on July 27, 2012 (No. 61/676,883).

35. Samsung had knowledge of the '608 Patent no later than August 2, 2021 via its access to Netlist's patent portfolio docket. Samsung has also gained knowledge of the '608 Patent via the Netlist's litigation against Samsung regarding a patent in the same family, U.S. Patent No. 10,860,506, which is a continuation of the '608 patent. Netlist filed the lawsuit on December 20, 2021. *Netlist, Inc. v. Samsung Elec. Co. Ltd., et. al.*, No. 21-cv-463-JRG Dkt. 1 (E.D. Tex. Dec. 20, 2021).

Samsung's Infringing Activities

36. ~~34.~~Samsung is responsible for making, using, selling, offering to sell, and/or importing, without authority, infringing DDR4 LRDIMMs ~~and~~, RDIMMs, and other products that have materially the same structures and designs in relevant part. Collectively, these are the "Accused Instrumentalities."

IV. FIRST CLAIM FOR RELIEF – '912 PATENT[1]

37. ~~35.~~ Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this ~~First~~Second Amended Complaint as if fully set forth herein.

38. ~~36.~~On information and belief, Samsung directly infringed and is currently infringing at least one claim of the '912 patent by, among other things, making, using,

[1] The claims asserted, and the theories set forth herein are based on Netlist's present understanding of Samsung's Accused Instrumentalities. Netlist reserves the right to supplement or amend these contentions as permitted by the Local Rules and any Orders of the Court as discovery progresses. Further, these contentions contain images and examples illustrating Netlist's infringement theories. As such, the images and examples are not intended, and should not be read, as narrowing or limiting the scope of these contentions.

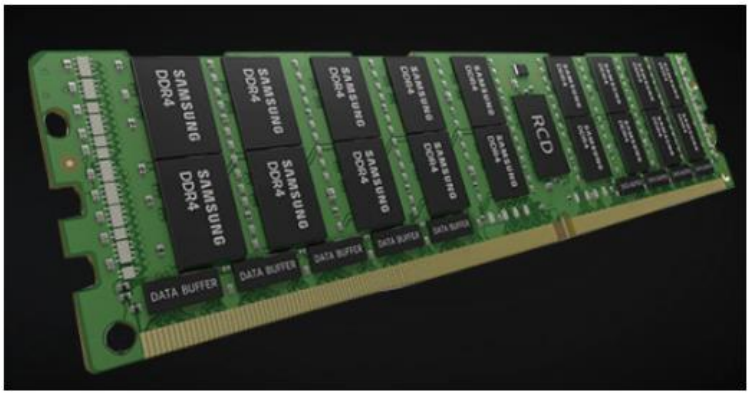
selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR4 LRDIMMs and DDR4 RDIMMs and other products with materially the same structures in relevant parts. For example, and as shown in Exhibit 5, the accused DDR4 LRDIMMs and DDR4 RDIMMs and other products with materially the same structures in relevant parts infringe at least claim 16 of the '912 patent. An exemplary claim chart comparing claim 16 of the '912 patent to exemplary Accused DDR4 LRDIMMs and RDIMMs products is attached as Exhibit 5.

V. SECOND CLAIM FOR RELIEF – '417 PATENT

39. ~~37.~~Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this ~~First~~**Second** Amended Complaint as if fully set forth herein.

40. ~~38.~~On information and belief, Defendants directly infringed and are currently infringing at least one claim of the '417 patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts. For example and as shown below, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts infringe at least claim 1 of the '417 patent.

41. ~~39.~~For example, to the extent the preamble is limiting, each of the accused DDR4 LRDIMMs comprise a memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide data bus in response to memory commands (e.g., read or write) received from the memory controller.

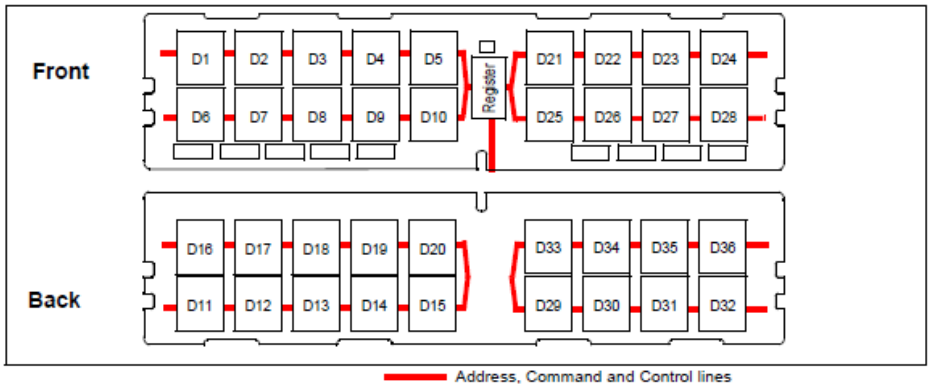


Load reduced DIMM

Include a register for enhancing clock, command and control signals
Enhanced data signal by placing data buffer
Best solution for achieving high density with high speed
Supports x4 Organization / up to 4 ranks per DIMM and 3DPC
Application : Server

(Depiction of an exemplary Samsung DDR4 LRDIMM advertised on its website, *available at* https://semiconductor.samsung.com/dram/module/lrdimm/m386a8k40bm1-crc/ (last accessed August 13, 2022)).

See also, e.g.,



NOTE :
1. CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2. CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3. Unless otherwise noted resistors are 22Ω ± 5%.

SAMSUNG

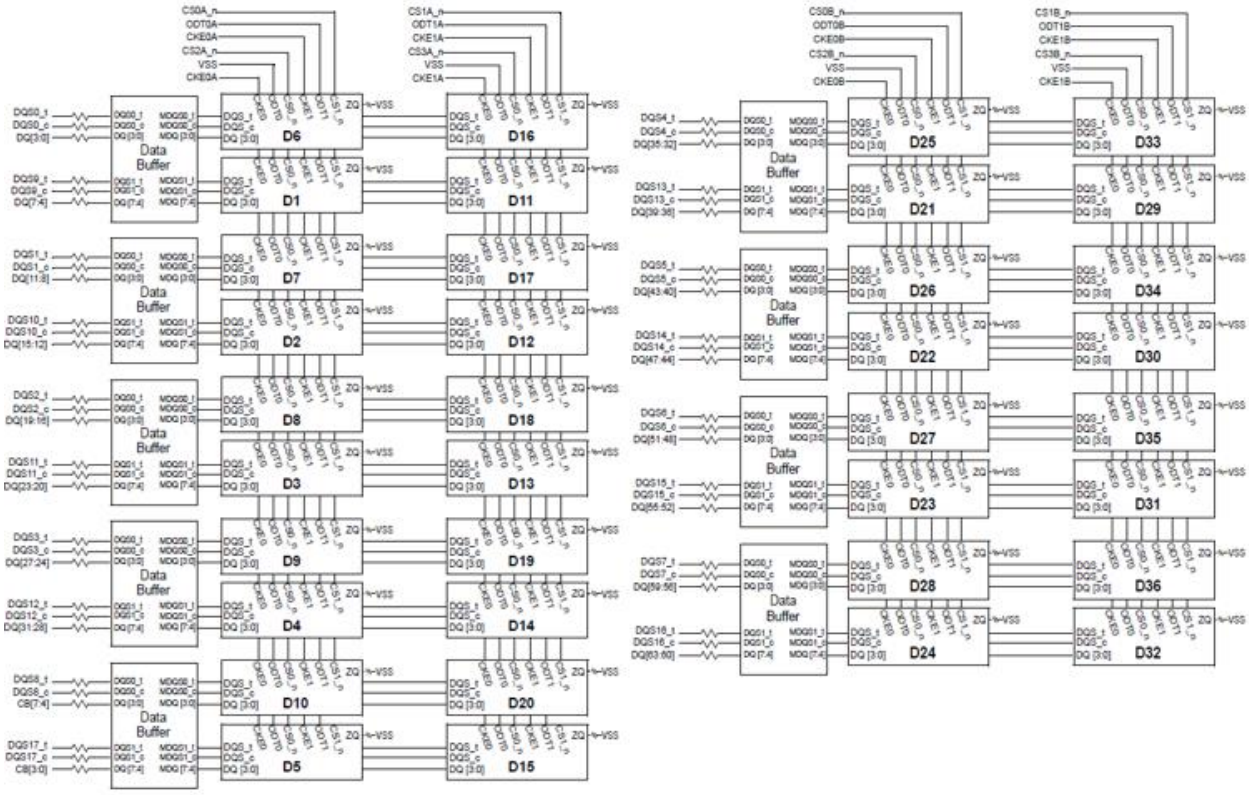
Exhibit 6 (datasheet for M386A8K40BM1-CRC) at 10;

5. Pin Description

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I2C serial bus clock for SPD/TS and register
BA0, BA1	Register bank select input	SDA	I2C serial bus data line for SPD/TS and register
BG0, BG1	Register bank group select input	SA0–SA2	I2C slave address select for SPD/TS and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	VPP	SDRAM activating power supply
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	Register clock enable lines input	VSS	Power supply return (ground)
ODT0, ODT1	Register on-die termination control lines input	VDDSPD	Serial SPD/TS positive power supply
ACT_n	Register input for activate input	ALERT_n	Register ALERT_n output
DQ0–DQ63	DIMM memory data bus	RESET_n	Set Register and SDRAMs to a Known State
CB0–CB7	DIMM ECC check bits	EVENT_n	SPD signals a thermal event has occurred
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)	VTT	SDRAM I/O termination supply
DQS0_c–DQS17_c	Data Buffer data strobes (negative line of differential pair)	RFU	Reserved for future use
CK0_t, CK1_t	Register clock input (positive line of differential pair)		
CK0_c, CK1_c	Register clocks input (negative line of differential pair)		

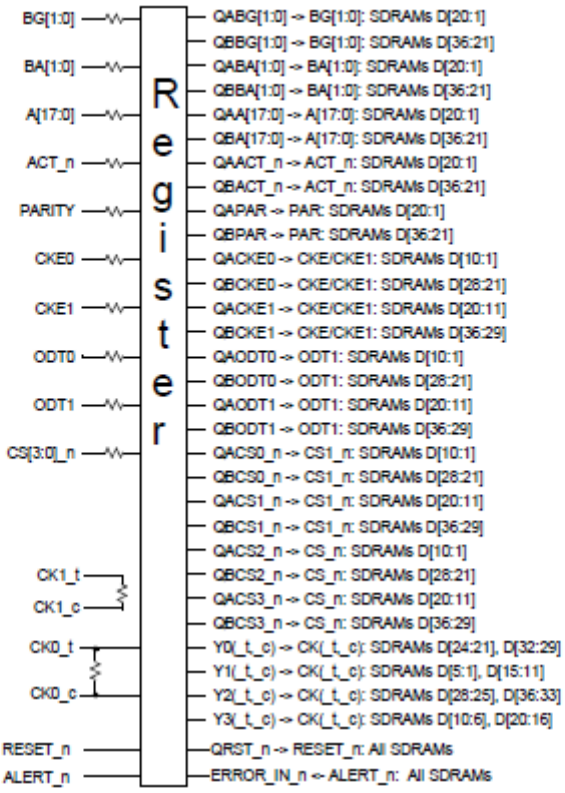
NOTE :
1. Address A17 is only valid for 16 Gb x4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

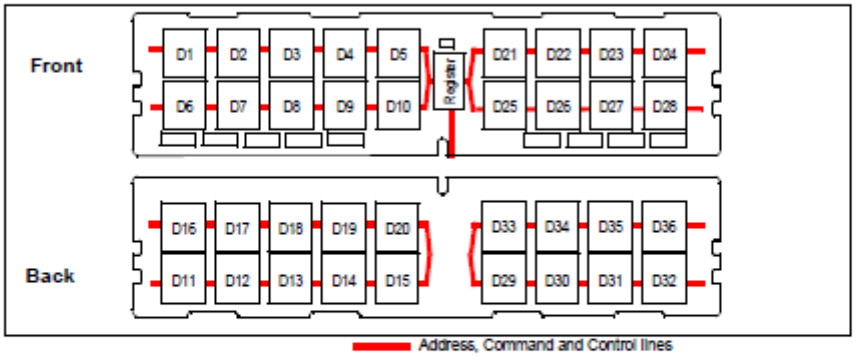
Id. at 6;



Id. at 11-12.

42. ~~40.~~As shown above and below, the memory bus includes address (e.g., "A[17:0]") and control signal lines (e.g., "CS[3:0]_n") and data signal lines (e.g., "DQ") connected via pins on the edge connection to the DIMM.



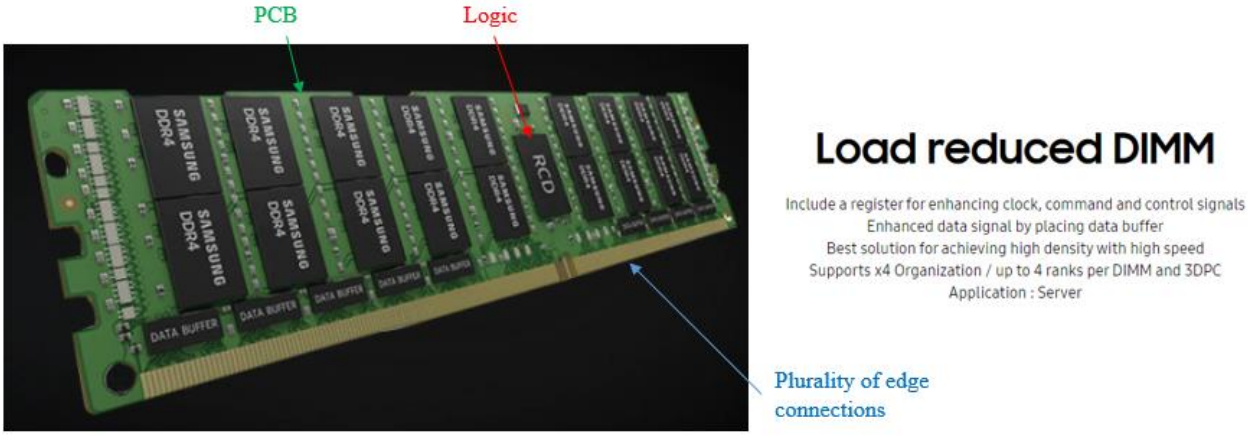


NOTE :
1. CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2. CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3. Unless otherwise noted resistors are 22Ω ± 5%.

SAMSUNG

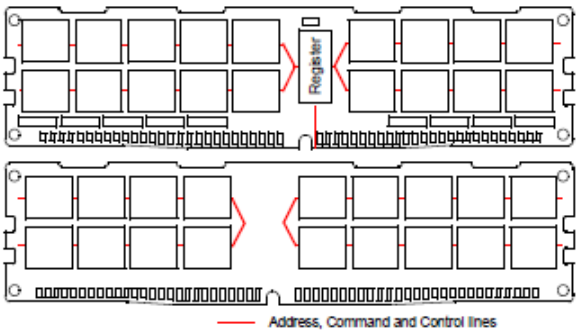
Exhibit 6 (datasheet for M386A8K40BM1-CRC) at 10.

43. ~~41.~~The accused DDR4 LRDIMMs each comprise a printed circuit board ("PCB") having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, with logic (e.g., DDR4 registering clock driver, or "RCD") coupled to the PCB.



(Annotated depiction of exemplary Samsung DDR4 LRDIMM advertised on its website, *available at* https://semiconductor.samsung.com/dram/module/lrdimm/m386a8k40bm1-crc/ (last accessed August 13, 2022)). *See also*, Exhibit 4 (Samsung Module Handling Guide depicting plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system):

18.1.1 x72 DIMM, populated as Quad physical ranks of x4 DDR4 SDRAMs



The used device is 4G x4(DDP) DDR4 SDRAM, FBGA.
DDR4 SDRAM Part NO: K4AAG045WB-MC**

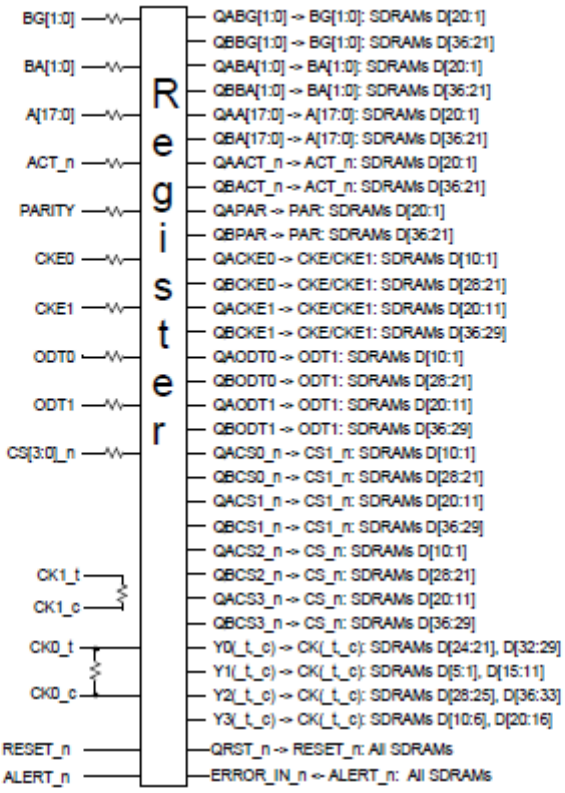
* NOTE : Tolerances on all dimensions ±0.15 unless otherwise specified.

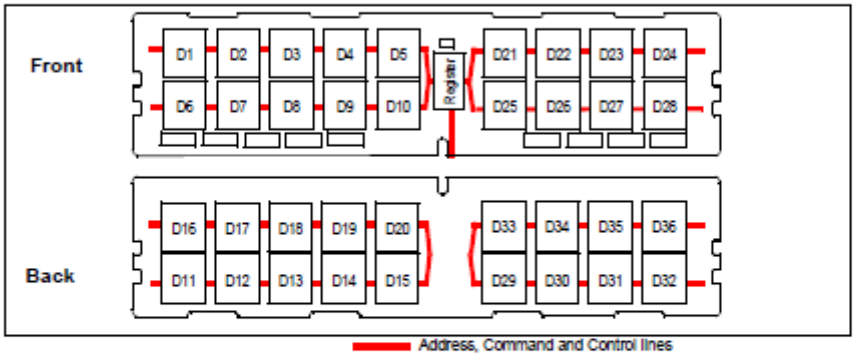
SAMSUNG

Exhibit 6 (datasheet for M386A8K40BM1-CRC) at 40.

44. ~~42.~~As shown below, the logic in each of the accused DDR4 LRDIMMs is configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals. The set of input address and control signals includes a plurality of input chip select signals and other input address and control signals. The plurality of input chip select signals include one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value. The logic receives the chip select signals with one active value and one or more chip selects with a non-active value and outputs corresponding registered chip selects. As shown below, the set of registered address and control signals output by the logic include a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other

input address and control signals. The plurality of registered chip select signals include one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value.





NOTE :

1. CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2. CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3. Unless otherwise noted resistors are 22Ω ± 5%.

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Exhibit 6 (datasheet for M386A8K40BM1-CRC) at 10.

7. Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE, are disabled during power-down. Input buffers,excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0, C1	Input	Chip ID : Chip ID is only used for 3DS for 2and4 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/, signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. For x8 device, the function of DM is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifing whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH.
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. For x4/x8 based SDRAMs, BG0 and BG1 are valid. For x16 based SDRAM components only BG0 is valid.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A16	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR4 SDRAMs support differential data strobe only and does not support single-ended.

Id. at 7 (input/output functional description for Samsung DDR4 LRDIMMs, including input address and control signals associated with a read or write memory command); *see*

also, e.g., JEDEC DDR4 SDRAM Standard 79-4C (Exhibit 8), at 29 (Command Truth Table providing input address and control signals associated with memory commands).

See also, e.g., JEDEC 82-31A RCD Standard (Exhibit 9), at 2-3 (detailing the three basic modes of operation of the DDR4 RCD; as explained in the JEDEC 82-31A RCD Standard, commands may be sent to a single rank, that is, one chip select has an active value, indicating that the selected rank is active, while the other one or more chip select signals have a non-active signal value):

Table 1 — Generic DCS - QxCS Mapping

Input CS	Output CS		
	Direct DualCS mode	Direct QuadCS mode	Encoded QuadCS mode
DCS0_n	QxCS0_n	QxCS0_n	QxCS0_n, QxCS1_n
DCS1_n	QxCS1_n	QxCS1_n	QxCS2_n, QxCS3_n
DCS2_n/DC0	n/a	QxCS2_n	n/a
DCS3_n/DC1	n/a	QxCS3_n	n/a

2.2.1 Direct CS Modes

Commands are sent to a single rank or multiple ranks, as determined by the DCS[n:0]_n and DC[n:0] inputs. The number of input chip selects matches the number of output chip selects in each of the two sets (A-outputs and B-outputs).

The number of input chip selects is two (in Direct DualCS mode) or four (in Direct QuadCS mode).

2.2.2 Quad CS Modes

For DIMMs using dual-die packages there is a need for four CS signals rather than the standard two. For these modules two modes are available where four CS outputs are available. The memory controller can select by programming the CS mode control bits which of the two modes it wants to utilize.

There are two ways of accomplishing this:

- by using four CS inputs from the host (DCS[3:0]_n). This is the Direct QuadCS mode. See Chapter 2.2.1, "Direct CS Modes," above.
- by using two CS inputs and one of the chip ID inputs from the host (DCS[1:0]_n and DC0). See Chapter 2.2.3, "Encoded QuadCS Mode," below.

2.2.3 Encoded QuadCS Mode

When F0RC0D DA[1:0] = 11 the DDR4 register decodes two sets of four QxCS_n outputs from two DCS_n inputs by using the DC0 as the encoding input.

Table 2 — DCS, DC - QxCS, QxC Mapping in Encoded QuadCS mode

DCS1_n	DCS0_n	DC0	DC2	QxCS[3:0]_n	QxC2
H	H	X	0	HHHH	No change
		X	1		
H	L	0	0	HHHL	0
		0	1		1
		1	0	HHLH	0
		1	1		1
L	H	0	0	HLHH	0
		0	1		1
		1	0	LHHH	0
		1	1		1
L	L	0	0	HLHL[1]	0
		0	1		1
		1	0	LHLH[1]	0
		1	1		1

1.Only one DCSx_n input can be asserted for DRAM MRS and DRAM read commands

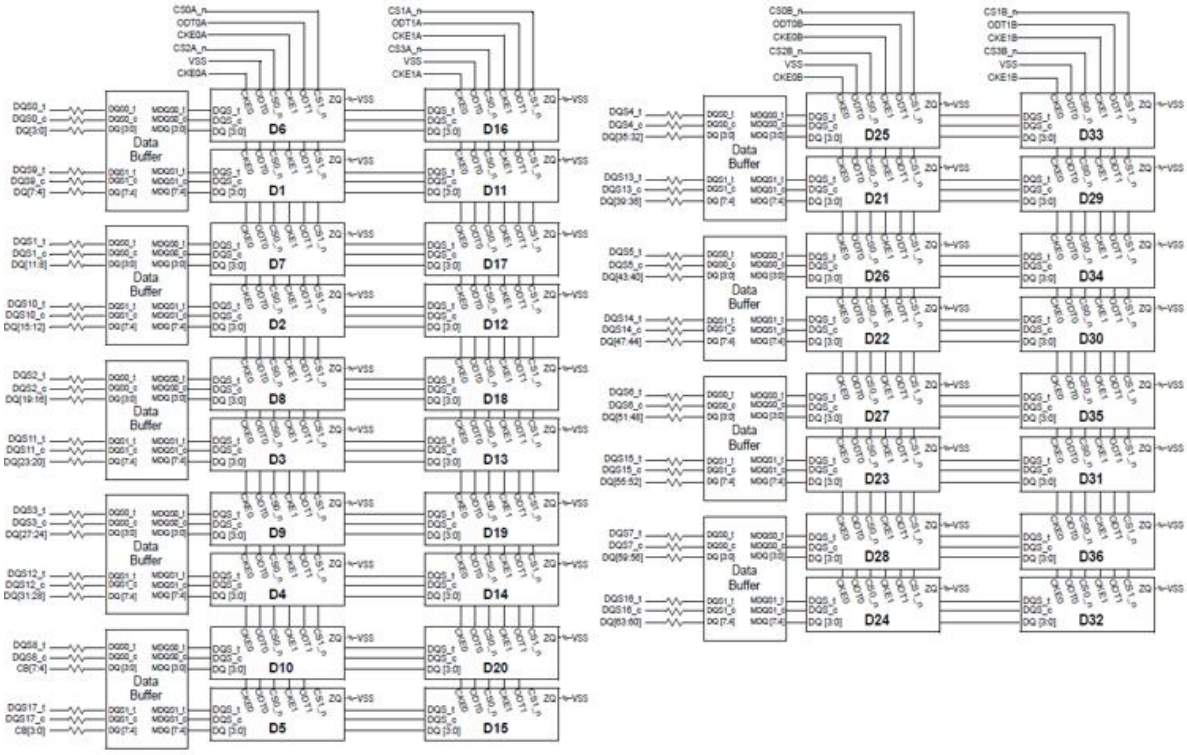


Exhibit 6 (datasheet for M386A8K40BM1-CRC) at 11-12.

45. ~~43.~~The logic is further configurable to output data buffer control signals (e.g., BCOM[3:0]=1001 or BCOM[3:0]=1000) in response to the read or write memory command, e.g., via the data buffer control bus BCOM[3:0] bus. *See, e.g.*, JEDEC 82-32A Data Buffer Standard (Exhibit 7), at 3-4:

2.4 Data Buffer Control Bus

This section describes the signals used in the DDR4 LRDIMM control bus that connects the DDR4 Register with each of the nine DDR4 data buffers (DDR4DB02).

2.4.1 Control Bus Signals

Table 2 — List of Signals for Data Buffer control

Name	Description	Signal Count
BCOM[3:0]	Data buffer command signals	4
BCKE	Function of registered DCKE (dedicated non-encoded signal)	1
BODT	Function of registered DODT (dedicated non-encoded signal)	1
BCK_t, BCK_c	Input clock	2
BVrefCA	Reference voltage for command and control signals	1
	Total	9

2.4.2 Command List

Table 3 — DDR4 Data Buffer Command Table

Command	Description	BCOM[3:0] Encoding
WR	Write BC4 or BC8 (fixed or on the fly) or BC10 (with CRC enabled) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1000
RD	Read BC4 or BC8 (fixed or on the fly) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1001
MRS Write	Send MRS Write bits snooped by DDR4 Register and the MRS ID in the following six command time slots, followed by parity in the last command time slot.	1011
BCW Write	Write buffer control word data in the next five command slots, followed by parity in the last command time slot.	1100
BCW Read	Read buffer control word address in the four command slots, followed by parity in the last command time slot.	1101
RFU[1]	Reserved for future use	1110
RFU[1]	Reserved for future use	1111
NOP	Idle, do nothing	1010

1. RFU commands are treated as NOP commands for command sequence error detection

46. ~~44.~~The accused DDR4 LRDIMMs further comprise memory devices (e.g., SDRAMs D1-D36 below) mounted on the PCB and arranged in a plurality of N-bit wide

ranks (e.g., four ranks depicted below), which correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices on respective N-bit wide ranks.

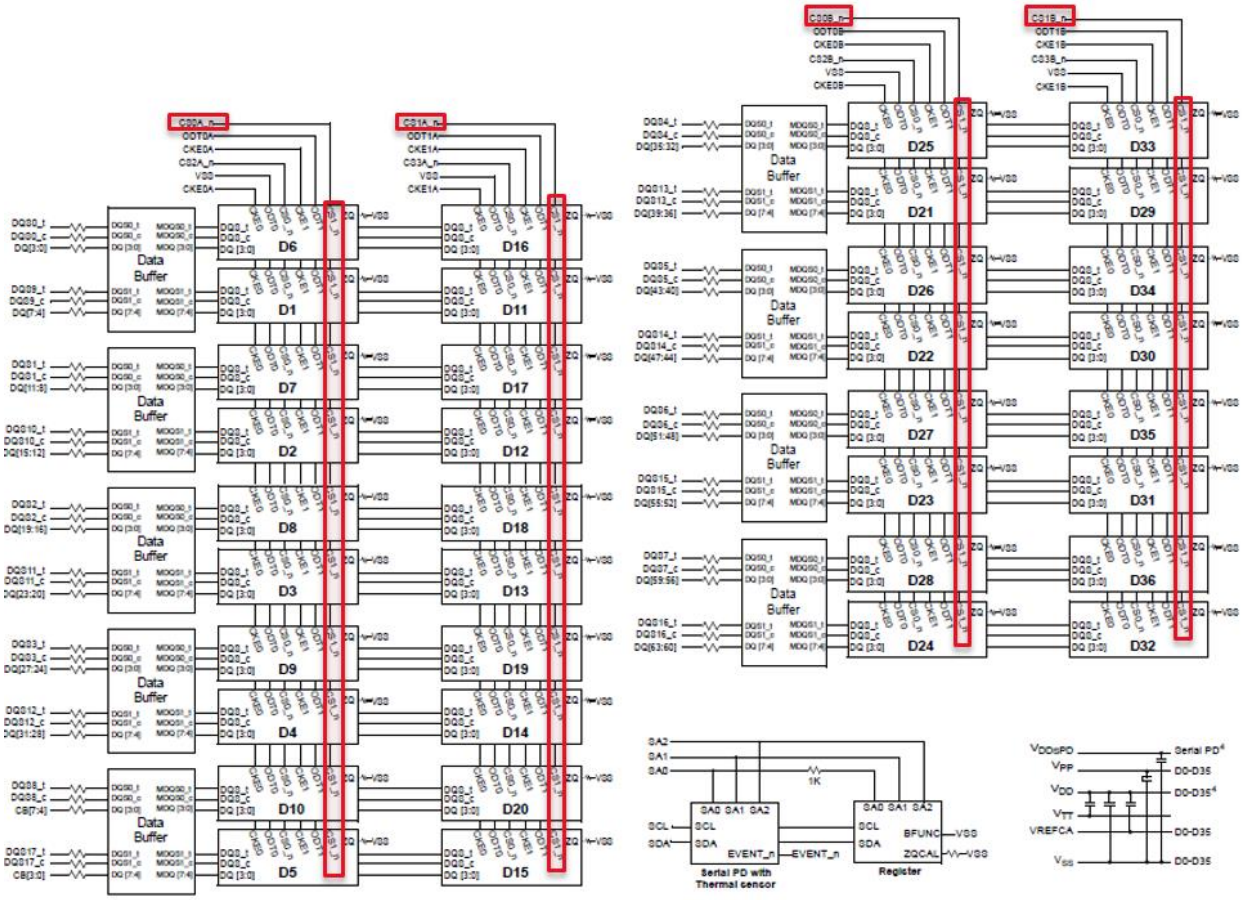
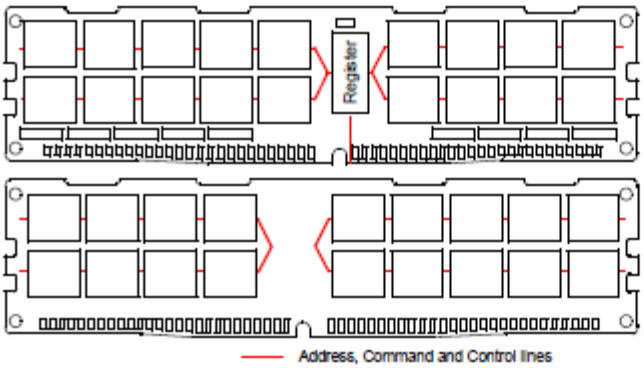


Exhibit 6 (datasheet for M386A8K40BM1-CRC) at 11-12.

18.1.1 x72 DIMM, populated as Quad physical ranks of x4 DDR4 SDRAMs



The used device is 4G x4(DDP) DDR4 SDRAM, FBGA.
DDR4 SDRAM Part NO: K4AAG045WB-MC**

* **NOTE** : Tolerances on all dimensions ±0.15 unless otherwise specified.

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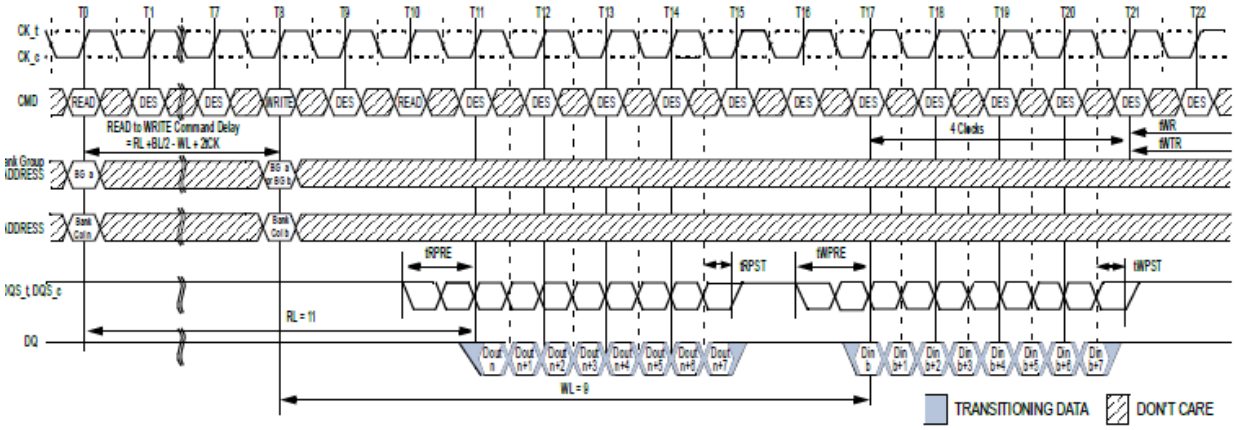
Id. at 40. *See also, e.g.*, JEDEC DDR4 SDRAM Standard 79-4C (Exhibit 8), at 105, 122 (examples of read/write burst operations):

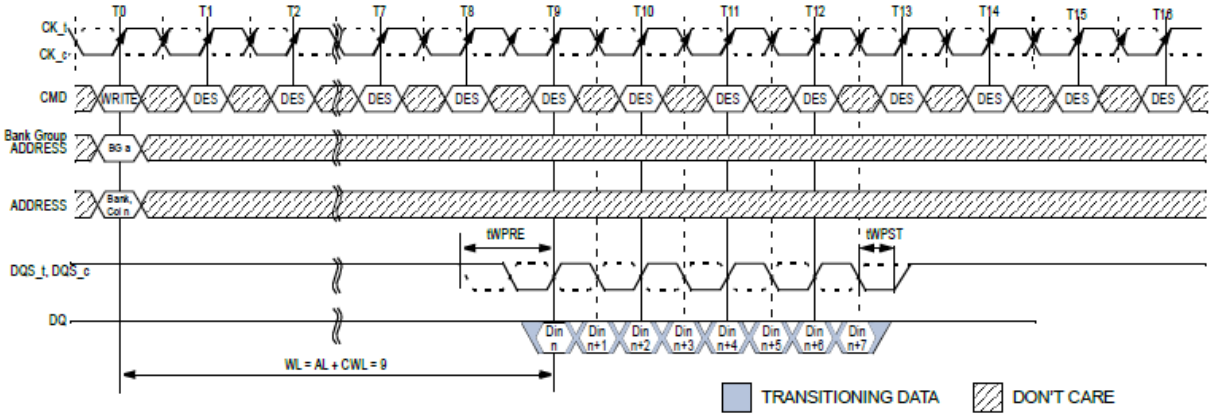


OTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL =9 (CWL = 9, AL = 0), Write Preamble = 1tCK
OTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.
OTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
OTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.
OTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 98 — READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group

4.25.5 Write Burst Operation

The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.
In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.



NOTE 1 BL = 8, WL = 9, AL = 0, CWL = 9, Preamble = 1tCK
NOTE 2 DIN n = data-in to column n.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

Figure 128 — WRITE Burst Operation WL = 9 (AL = 0, CWL = 9, BL8)

47. ~~45.~~The accused DDR4 LRDIMMs each include circuitry (e.g., DDR4 data buffers) coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks.

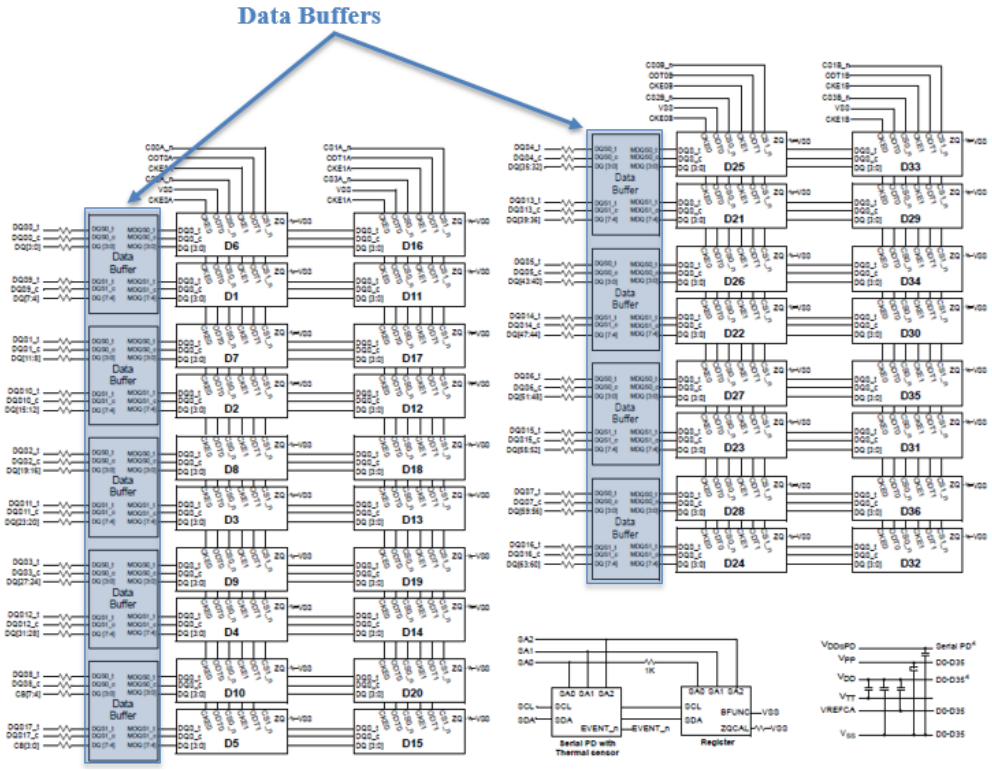


Exhibit 6 (datasheet for M386A8K40BM1-CRC) at 11-12.

4.61 Logic Diagram

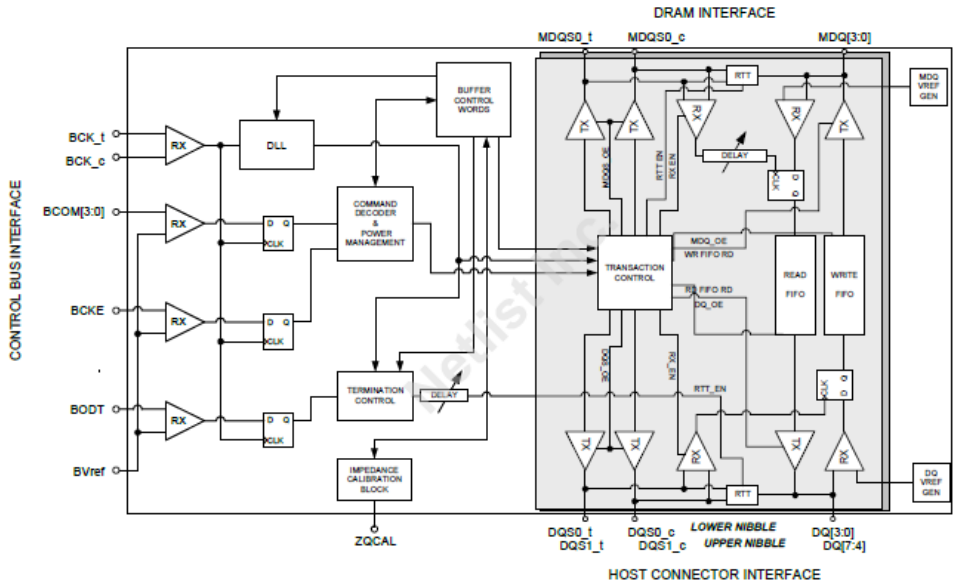


Figure 15 — Logic Diagram

JEDEC 82-32A Data Buffer Standard (Exhibit 7), at 95 (exemplary logic diagram of DDR4 data buffer circuitry).

48. ~~46.~~In each of the accused DDR4 LRDIMMs, the circuitry (e.g., DDR4 data buffer) is configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals (e.g., BCOM[3:0]=1001 or BCOM[3:0]=1000) and in accordance with an overall CAS latency of the memory module. *See, e.g.*, JEDEC 82-32A Data Buffer Standard (Exhibit 7), at 12, 14:

Table 4 — Multicycle Sequence for Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	WR	Write command BCOM[3:0] = 1000
2	DAT0	Transfer the rank ID for write command BCOM[1:0] = {RANK_ID[1:0]} for DRAM writes Burst length information for Write data BCOM[3:2] = {0, 0} for BC4 BCOM[3:2] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for WR command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

Table 5 — Multi-cycle Sequence for Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	RD	Read command BCOM[3:0] = 1001
2	DAT0	Transfer the rank ID for read command or the MPR selection ID in MPR override read mode BCOM[1:0] = {RANK_ID[1:0]} for DRAM reads BCOM[1:0] = {BA1, BA0} for MPR override reads Burst length information for Read data BCOM[3:0] = {0, 0} for BC4[1] BCOM[3:0] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for RD command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

1. BC4 is not supported for MPR override reads

The overall CAS latency of the memory module may be expressed as shown below in the following equations:

2.5.4 Command Sequence Descriptions

The timing diagrams in this section show only the lower nibble of the DDR4RCD02. The same timing relationships apply independently also for the upper nibble. The timing diagrams only show the case of burst length = 8 and preamble = 1 nCK but equivalent timing relationships exist for burst length = 4 & 10 and preamble = 2 nCK.

For readability reasons, the timing diagrams use the abbreviations DB_RL and DB_WL for the latency between first cycle of RD command and the first rising edge of MDQS at DDR4DB02 inputs and for the latency between first cycle of WR command and the first rising edge of MDQS at DDR4DB02 outputs respectively. Both DB_RL and DB_WL include full cycle and fractional cycle delays. The equations for these latencies are as follows:

$DB\_WL(R)^1 = CWL + AL + PL + DWL(R)$

$DB\_RL(R)^2 = CL + AL + PL + MRE(R) + tRPRE/2$

tRPRE/2 exists in DB_RL since the host will adjust the receive enable delay MRE(R) to place it in the center of the read preamble.

For the detailed equations for DWL and MRE refer to the DDR4DB02 specification.

The DDR4RCD02 delays tPDM_RD and tPDM_WR are defined as the delay between first rising edge of MDQS and the first rising edge of DQS for a RD command and as the delay between first rising edge of DQS and the first rising edge of MDQS for a WR command respectively. By default these delays are constant per DDR4RCD02 for all ranks and nibbles.

---

1. This equation assumes that the DDR4 data buffer MDQ-MDQS Write Delay Control Words in F[3:0]BC8x/ F[3:0]BC9x are at their default power-on setting.
2. This equation assumes that the DDR4 data buffer MDQS Read Delay Control Words in F[3:0]BC4x/ F[3:0]BC5x are at their default power-on setting.

JEDEC 82-31A RCD Standard (Exhibit 9), at 15.

49. ~~47.~~The data transfers through the circuitry (e.g., DDR4 data buffer) are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices. As an example, the overall CAS latency of the memory module may be expressed as shown below.

See, e.g., 82-32A Data Buffer Standard (Exhibit 7), at 11-12:

2.12 Command Sequence Descriptions

To accommodate the worst case DRAM CAS Latency, Additive Latency and Parity Latency, a DB is required to support a queue depth of 12 commands on the BCOM bus for data rates up to 2400MT/s.

The timing diagrams in this section show only the lower nibble of the DDR4DB02. The same timing relationships apply independently also for the upper nibble. The timing diagrams only show the case of burst length = 8 and preamble = 1 nCK but equivalent timing relationships exist for burst length = 4 & 10 and preamble = 2 nCK.

For readability reasons, the timing diagrams use the abbreviations DB_RL and DB_WL for the latency between first cycle of RD command and the first rising edge of MDQS at DDR4DB02 inputs and for the latency between first cycle of WR command and the first rising edge of MDQS at DDR4DB02 outputs respectively. Both DB_RL and DB_WL include full cycle and fractional cycle delays. The equations for these latencies are as follows:

$DB\_WL(R)^1 = CWL + AL + PL + DWL(R)$

$DB\_RL(R)^2 = CL + AL + PL + MRE(R) + tRPRE/2$

The equations for DWL and MRE for Ranks 0 to 3 are listed below.

where xxx[R].l and xxx[R].u are the equations for the lower and upper nibbles respectively

DWL[0].l = (F0BCDx[2:0] * 64 + F0BCAx[5:0]) * tCK/64

DWL[0].u = (F0BCDx[6:4] * 64 + F0BCBx[5:0]) * tCK/64

DWL[1].l = (F1BCDx[2:0] * 64 + F1BCAx[5:0]) * tCK/64

DWL[1].u = (F1BCDx[6:4] * 64 + F1BCBx[5:0]) * tCK/64

DWL[2].l = (F0BCFx[2:0] * 64 + F2BCAx[5:0]) * tCK/64

DWL[2].u = (F0BCFx[6:4] * 64 + F2BCBx[5:0]) * tCK/64

DWL[3].l = (F1BCFx[2:0] * 64 + F3BCAx[5:0]) * tCK/64

DWL[3].u = (F1BCFx[6:4] * 64 + F3BCBx[5:0]) * tCK/64

MRE[0].l = (F0BCCx[2:0] * 64 + F0BC2x[5:0]) * tCK/64

MRE[0].u = (F0BCCx[6:4] * 64 + F0BC3x[5:0]) * tCK/64

MRE[1].l = (F1BCCx[2:0] * 64 + F1BC2x[5:0]) * tCK/64

MRE[1].u = (F1BCCx[6:4] * 64 + F1BC3x[5:0]) * tCK/64

MRE[2].l = (F0BCEx[2:0] * 64 + F2BC2x[5:0]) * tCK/64

MRE[2].u = (F0BCEx[6:4] * 64 + F2BC3x[5:0]) * tCK/64

MRE[2].l = (F1BCEx[2:0] * 64 + F3BC2x[5:0]) * tCK/64

MRE[2].u = (F1BCEx[6:4] * 64 + F3BC3x[5:0]) * tCK/64

tRPRE/2 exists in DB_RL since the host will adjust the receive enable delay MRE(R) to place it in the center of the read preamble.

The DDR4DB02 delays tPDM_RD and tPDM_WR are defined as the delay between first rising edge of MDQS and the first rising edge of DQS for a RD command and as the delay between first rising edge of DQS and the first rising edge of MDQS for a WR command respectively. By default these delays are constant per DDR4DB02 for all ranks and nibbles.

50. ~~48.~~On information and belief, Samsung also indirectly infringes the '417 patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Samsung's customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has induced, and currently induces, the infringement of the '417 patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR4 LRDIMM products and other materially similar products that infringe the '417 patent. On information and belief, Samsung provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR4 LRDIMM products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

51. ~~49.~~On information and belief, Samsung also indirectly infringes the '417 patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has contributed to, and currently contributes to, Samsung's customers and end-users infringement of the '417 patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR4 LRDIMM products and other materially similar products that infringe the '417 patent. On information and belief, the accused DDR4 LRDIMM and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Samsung is aware that

the product or process that includes the accused DDR4 LRDIMM products and other materially similar products would be covered by one or more claims of the '417 patent. On information and belief, the use of the product or process that includes the accused DDR4 LRDIMM products infringes at least one claim of the '417 patent.

52. ~~50.~~Samsung's infringement of the '417 patent has damaged and will continue to damage Netlist. Samsung has had actual notice of the application that issued as the '417 patent since at least August 2, 2021. Samsung's infringement of the '417 patent has been continuing and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

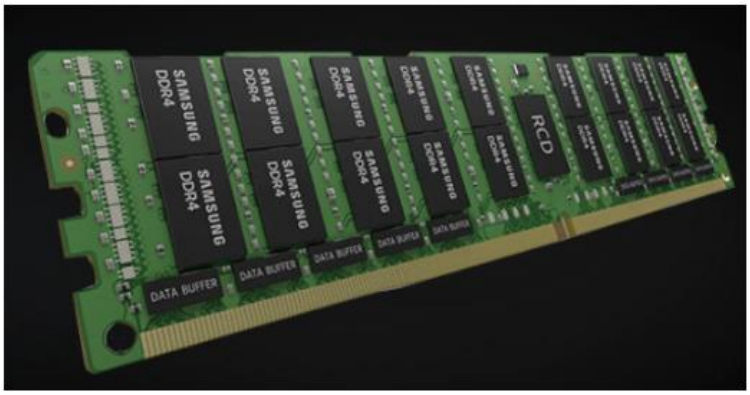
VI. THIRD CLAIM FOR RELIEF – '215 PATENT

53. ~~51.~~Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this ~~First~~Second Amended Complaint as if fully set forth herein.

54. ~~52.~~On information and belief, Defendants directly infringed and are currently infringing at least one claim of the '215 patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts. For example and as shown below, the accused DDR4 LRDIMMs and other products with materially the same structures in relevant parts infringe at least claim 1 of the '215 patent.

55. ~~53.~~For example, to the extent the preamble is limiting, the accused DDR4 LRDIMMs comprise a memory module operable in a computer system to communicate

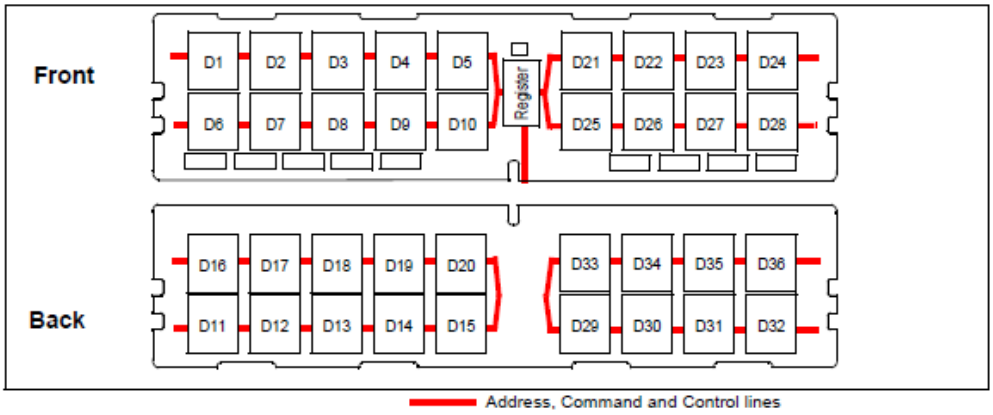
data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller.



Load reduced DIMM

Include a register for enhancing clock, command and control signals
Enhanced data signal by placing data buffer
Best solution for achieving high density with high speed
Supports x4 Organization / up to 4 ranks per DIMM and 3DPC
Application : Server

(Depiction of an exemplary Samsung DDR4 LRDIMM advertised on its website, *available at* https://semiconductor.samsung.com/dram/module/lrdimm/m386a8k40bm1-crc/ (last accessed August 13, 2022)).



NOTE :
1. CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2. CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3. Unless otherwise noted resistors are 22Ω ± 5%.

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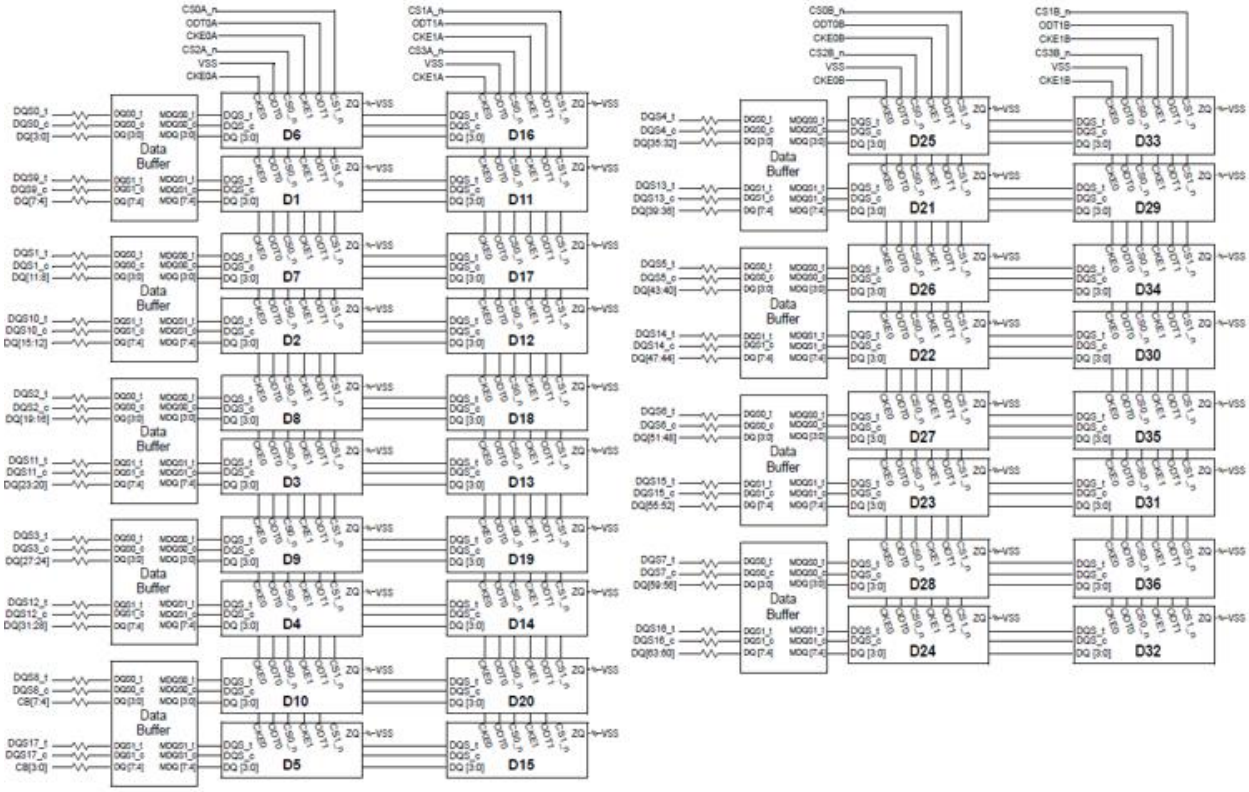
Exhibit 6 (datasheet for M386A8K40BM1-CRC) at 10.

5. Pin Description

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I2C serial bus clock for SPD/TS and register
BA0, BA1	Register bank select input	SDA	I2C serial bus data line for SPD/TS and register
BG0, BG1	Register bank group select input	SA0–SA2	I2C slave address select for SPD/TS and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	VPP	SDRAM activating power supply
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	Register clock enable lines input	VSS	Power supply return (ground)
ODT0, ODT1	Register on-die termination control lines input	VDDSPD	Serial SPD/TS positive power supply
ACT_n	Register input for activate input	ALERT_n	Register ALERT_n output
DQ0–DQ63	DIMM memory data bus	RESET_n	Set Register and SDRAMs to a Known State
CB0–CB7	DIMM ECC check bits	EVENT_n	SPD signals a thermal event has occurred
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)	VTT	SDRAM I/O termination supply
DQS0_c–DQS17_c	Data Buffer data strobes (negative line of differential pair)	RFU	Reserved for future use
CK0_t, CK1_t	Register clock input (positive line of differential pair)		
CK0_c, CK1_c	Register clocks input (negative line of differential pair)		

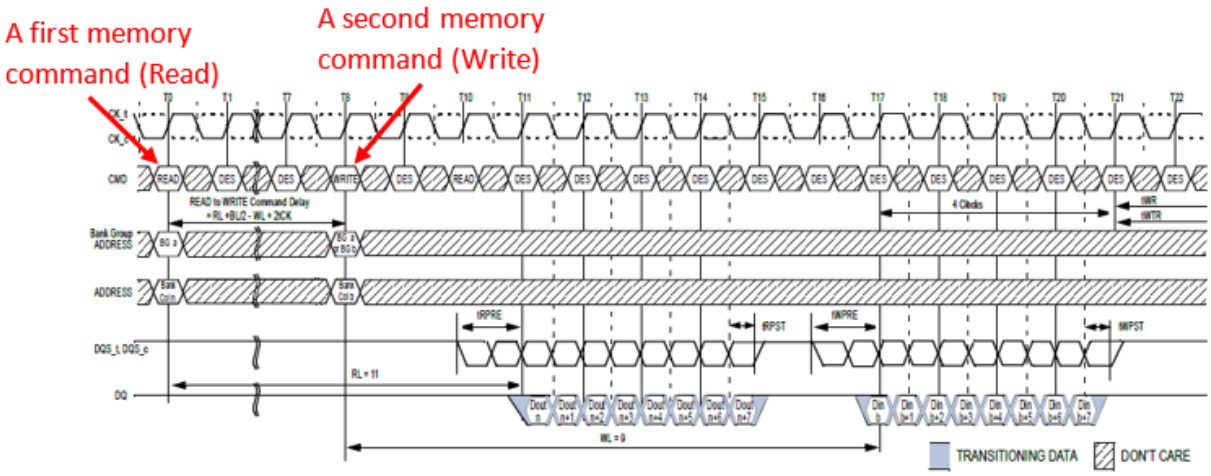
NOTE :
1. Address A17 is only valid for 16 Gb x4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

Id. at 6.


CS0A_n
ODT0A
CKE0A
CS2A_n
VSS
CKE0A
CS1A_n
ODT1A
CKE1A
CS3A_n
VSS
CKE1A
Data Buffer
D6
D16
D1
D11
D7
D17
D2
D12
D8
D18
D3
D13
D9
D19
D4
D14
D10
D20
D5
D15
CS0B_n
ODT0B
CKE0B
CS2B_n
VSS
CKE0B
CS1B_n
ODT1B
CKE1B
CS3B_n
VSS
CKE1B
D25
D33
D21
D29
D26
D34
D22
D30
D27
D35
D23
D31
D28
D36
D24
D32
ZQ
VSS

Id. at 11-12.

56. ~~54.~~The memory commands may include a first memory command and a subsequent second memory command, where the first memory command causes the memory module to receive or output a first data burst, and the second memory command causes the memory module to receive or output a second data burst, for example, as illustrated in the exemplary waveform and timing diagrams below.

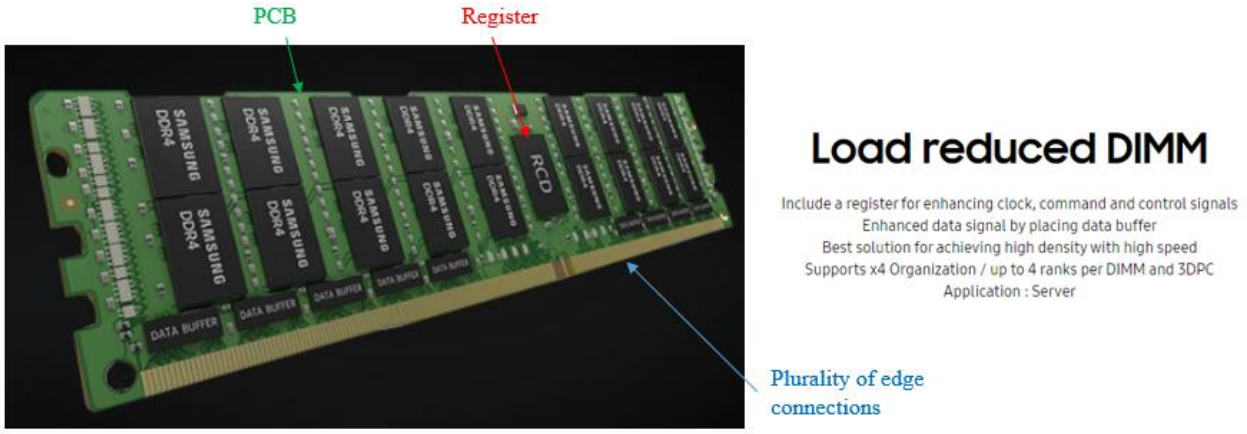


NOTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL =9 (CWL = 9, AL = 0), Write Preamble = 1tCK
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 98 — READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group

JEDEC DDR4 SDRAM Standard 79-4C (Exhibit 8), at 105; *see also, e.g.*, *id.*, §§ 4.24-4.25 (waveform and timing diagrams for JEDEC-standardized read and write operations).

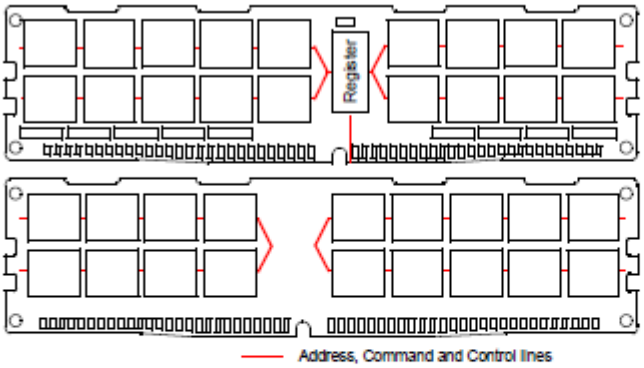
57. ~~55.~~The accused DDR4 LRDIMMs each include a PCB having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, and a register coupled to the PCB.



(Annotated depiction of an exemplary Samsung DDR4 LRDIMM advertised on its website, *available at* https://semiconductor.samsung.com/dram/module/lrdimm/m386a8k40bm1-crc/~~(last~~ **(last** accessed August 13, 2022)). *See also*, Exhibit 4 (Samsung Module Handling Guide depicting plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system):

See also, e.g., (datasheet for M386A8K40BM1-CRC) Exhibit 6 at 40:

18.1.1 x72 DIMM, populated as Quad physical ranks of x4 DDR4 SDRAMs



The used device is 4G x4(DDP) DDR4 SDRAM, FBGA.
DDR4 SDRAM Part NO: K4AAG045WB-MC**

* NOTE : Tolerances on all dimensions ±0.15 unless otherwise specified.

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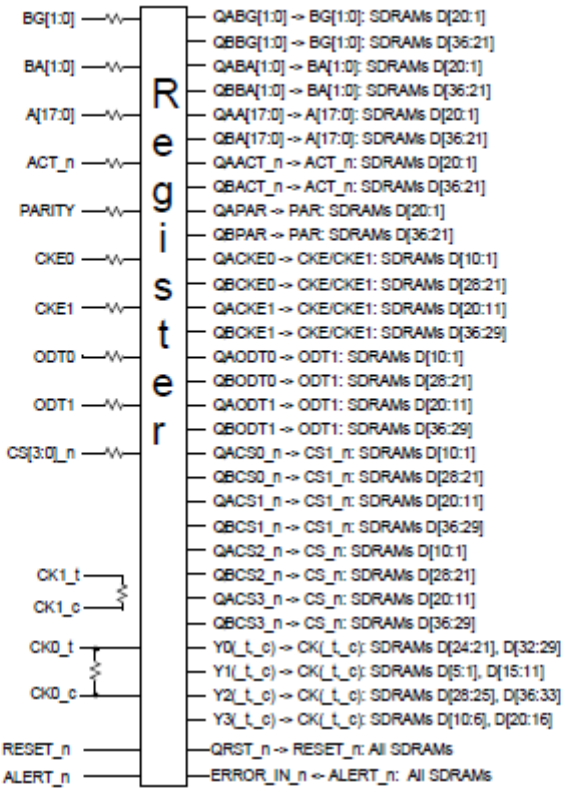
58. ~~56.~~ The register of each of the accused DDR4 LRDIMMs is configured to receive and buffer first command and address signals representing the first memory

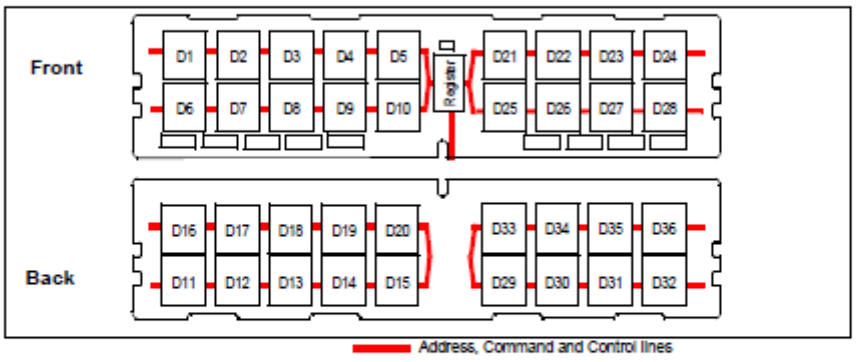
command, and to receive and buffer second command and address signals representing the second memory command.

7. Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE, are disabled during power-down. Input buffers,excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0, C1	Input	Chip ID : Chip ID is only used for 3DS for 2and4 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/, signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. For x8 device, the function of DM is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifing whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH.
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. For x4/x8 based SDRAMs, BG0 and BG1 are valid. For x16 based SDRAM components only BG0 is valid.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A16	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR4 SDRAMs support differential data strobe only and does not support single-ended.

Exhibit 6 (datasheet for M386A8K40BM1-CRC) at 7 (input/output functional description for Samsung DDR4 LRDIMMs, including command and address signals representing memory commands); *see also*, *e.g.*, JEDEC DDR4 SDRAM Standard 79-4C (Exhibit 8), at 29 (Command Truth Table providing command and address signals associated with memory commands).





NOTE :

1. CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2. CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3. Unless otherwise noted resistors are 22Ω ± 5%.

Id. at 10 (illustrating register receiving and buffering first command and address signals representing the first memory command and second command and address signals representing the second memory command).

59. ~~57.~~The accused DDR4 LRDIMMs each include a plurality of memory integrated circuits (e.g., SDRAMs, highlighted in blue below) mounted on the PCB and arranged in a plurality of ranks including a first rank and a second rank. The plurality of memory integrated circuits include at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank.

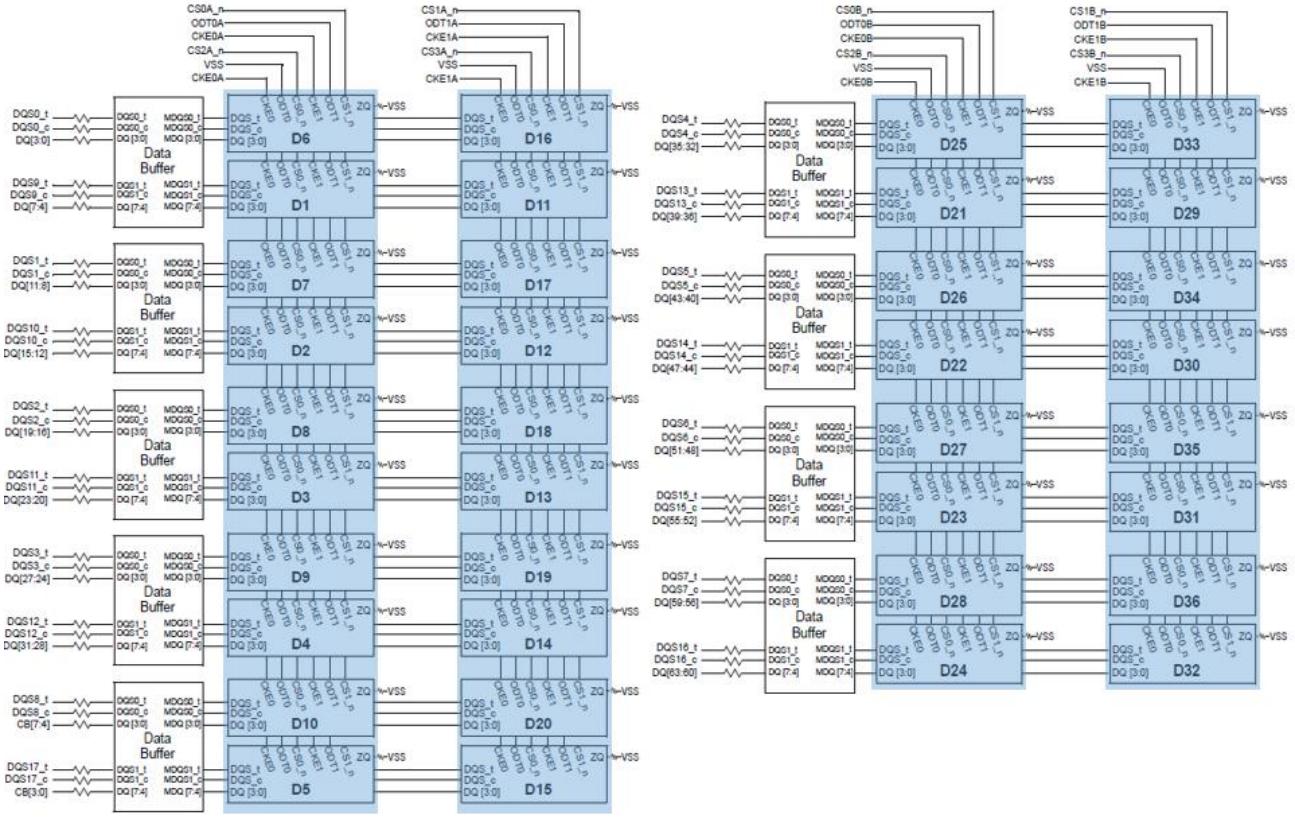
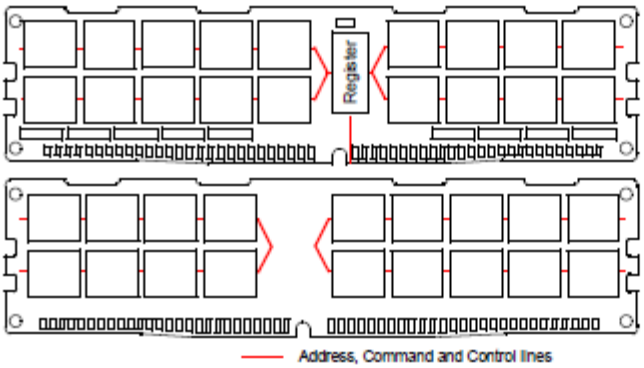


Exhibit 6 (datasheet for M386A8K40BM1-CRC) at 11-12.

18.1.1 x72 DIMM, populated as Quad physical ranks of x4 DDR4 SDRAMs

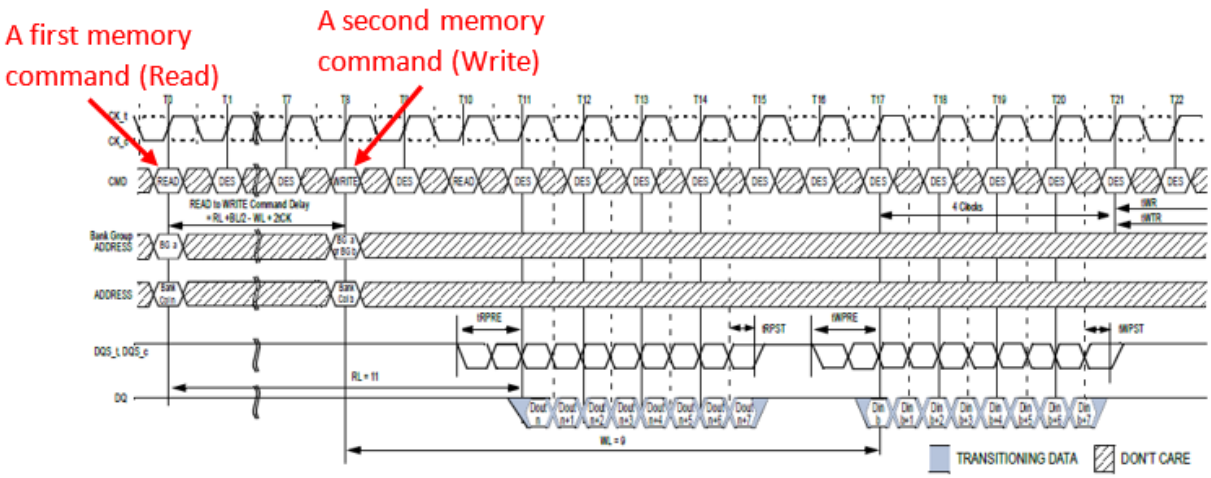


The used device is 4G x4(DDP) DDR4 SDRAM, FBGA.
DDR4 SDRAM Part NO: K4AAG045WB-MC**

* NOTE : Tolerances on all dimensions ±0.15 unless otherwise specified.

Id. at 40.

60. ~~58.~~As demonstrated in the exemplary waveform and timing diagram below, a first rank is selected to receive or output the first data burst in response to the first memory command, which is associated with a first chip-select signal, and is not selected to communicate data with the memory controller in response to the second memory command. Similarly, the second rank is selected to receive or output the second data burst in response to the second memory command, which is associated with a second chip-select signal, and is not selected to communicate data with the memory controller in response to the first memory command.



NOTE 1 BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL =9 (CWL = 9, AL = 0), Write Preamble = 1tCK
NOTE 2 DOUT n = data-out from column n, DIN b = data-in to column b.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 98 — READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group

JEDEC DDR4 SDRAM Standard 79-4C (Exhibit 8), at 105; *see also, e.g., id.*, §§ 4.24-4.25 (waveform and timing diagrams for JEDEC-standardized read and write operations); *see also, e.g.*, Exhibit 6 (datasheet for M386A8K40BM1-CRC) at 7 ("CS_n provides for external Rank selection on systems with multiple Ranks."); JESD 82-31A (Exhibit 9), at 2-3 (detailing the three basic modes of operation of the DDR4 RCD).

61. ~~59.~~ The accused DDR4 LRDIMMs further comprise a buffer (e.g. DDR4 data buffer) coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus.

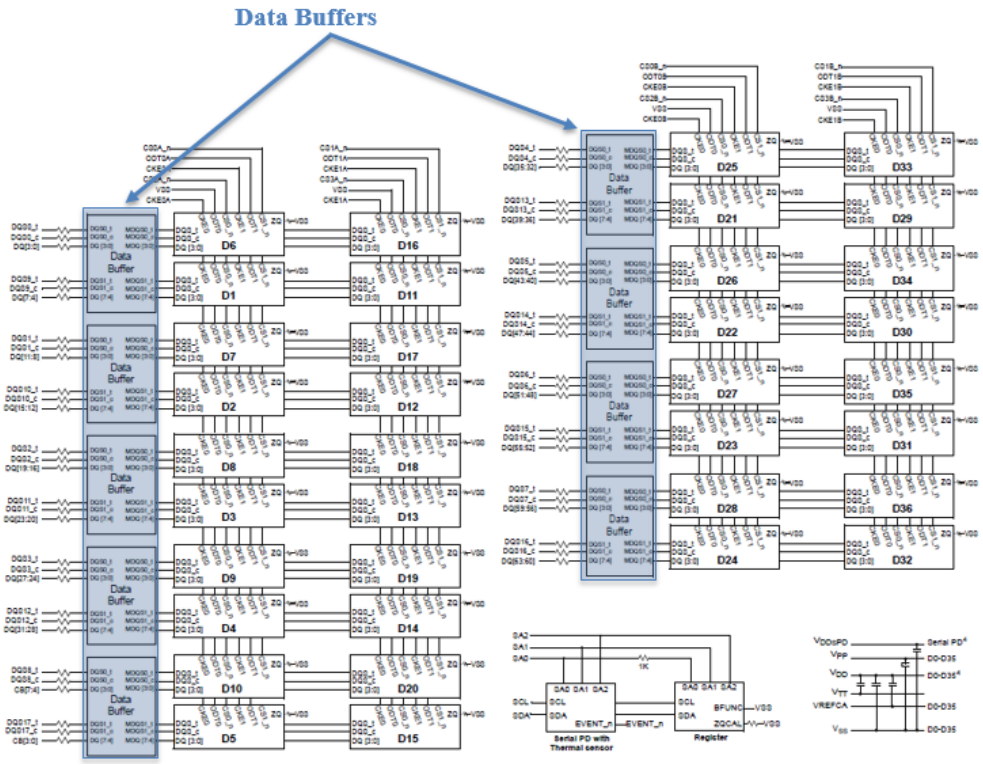


Exhibit 6 (datasheet for M386A8K40BM1-CRC) at 11-12.

4.61 Logic Diagram

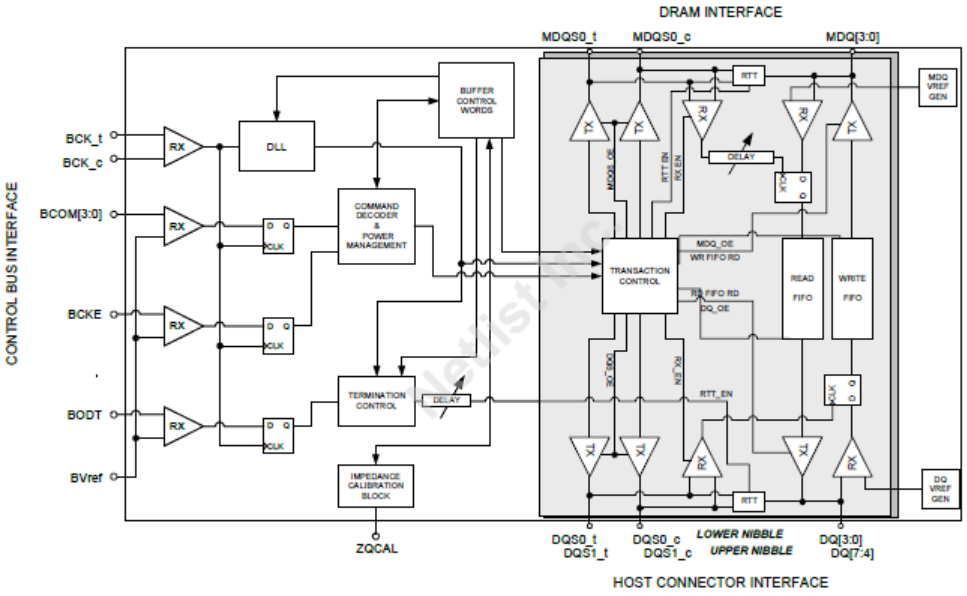


Figure 15 — Logic Diagram

JEDEC 82-32A Data Buffer Standard (Exhibit 7), at 95 (exemplary logic diagram of DDR4 data buffer circuitry).

62. ~~60.~~ As shown above and below, the buffer in each of the accused DDR4 LRDIMMs includes logic coupled to the buffer that is configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer. The logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.

2.4 Data Buffer Control Bus

This section describes the signals used in the DDR4 LRDIMM control bus that connects the DDR4 Register with each of the nine DDR4 data buffers (DDR4DB02).

2.4.1 Control Bus Signals

Table 2 — List of Signals for Data Buffer control

Name	Description	Signal Count
BCOM[3:0]	Data buffer command signals	4
BCKE	Function of registered DCKE (dedicated non-encoded signal)	1
BODT	Function of registered DODT (dedicated non-encoded signal)	1
BCK_t, BCK_c	Input clock	2
BVrefCA	Reference voltage for command and control signals	1
	Total	9

2.4.2 Command List

Table 3 — DDR4 Data Buffer Command Table

Command	Description	BCOM[3:0] Encoding
WR	Write BC4 or BC8 (fixed or on the fly) or BC10 (with CRC enabled) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1000
RD	Read BC4 or BC8 (fixed or on the fly) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1001
MRS Write	Send MRS Write bits snooped by DDR4 Register and the MRS ID in the following six command time slots, followed by parity in the last command time slot.	1011
BCW Write	Write buffer control word data in the next five command slots, followed by parity in the last command time slot.	1100
BCW Read	Read buffer control word address in the four command slots, followed by parity in the last command time slot.	1101
RFU[1]	Reserved for future use	1110
RFU[1]	Reserved for future use	1111
NOP	Idle, do nothing	1010

1. RFU commands are treated as NOP commands for command sequence error detection

JEDEC 82-32A Data Buffer Standard (Exhibit 7), at 3-4.

Table 4 — Multicycle Sequence for Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	WR	Write command BCOM[3:0] = 1000
2	DAT0	Transfer the rank ID for write command BCOM[1:0] = {RANK_ID[1:0]} for DRAM writes Burst length information for Write data BCOM[3:2] = {0, 0} for BC4 BCOM[3:2] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for WR command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

Table 5 — Multi-cycle Sequence for Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	RD	Read command BCOM[3:0] = 1001
2	DAT0	Transfer the rank ID for read command or the MPR selection ID in MPR override read mode BCOM[1:0] = {RANK_ID[1:0]} for DRAM reads BCOM[1:0] = {BA1, BA0} for MPR override reads Burst length information for Read data BCOM[3:0] = {0, 0} for BC4[1] BCOM[3:0] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for RD command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

1. BC4 is not supported for MPR override reads

Id. at 12, 14.

63. ~~61.~~On information and belief, Samsung also indirectly infringes the '215 patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as

Samsung's customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has induced, and currently induces, the infringement of the '215 patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR4 LRDIMM products and other materially similar products that infringe the '215 patent. On information and belief, Samsung provides specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR4 LRDIMM products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

64. ~~62.~~On information and belief, Samsung also indirectly infringes the '215 patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has contributed to, and currently contributes to, Samsung's customers and end-users infringement of the '215 patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR4 LRDIMM products and other materially similar products that infringe the '215 patent. On information and belief, the accused DDR4 LRDIMM and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Samsung is aware that the product or process that includes the accused DDR4 LRDIMM products and other materially similar products would be covered by one or more claims of the '215 patent.

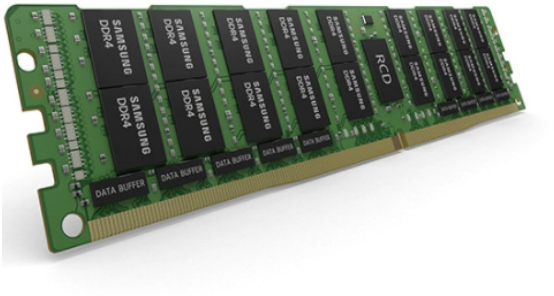
On information and belief, the use of the product or process that includes the accused DDR4 LRDIMM products infringes at least one claim of the '215 patent.

65. ~~**63.**~~Samsung's infringement of the '215 patent has damaged and will continue to damage Netlist. ~~**Samsung has had actual notice of the '215 patent since at least August 2, 2021. Samsung's infringement of the '215 patent has been continuing and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.**~~ **Samsung has had actual notice of the '215 patent since at least August 2, 2021. Samsung's infringement of the '215 patent has been continuing and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.**

VII. FOURTH CLAIM FOR RELIEF – '608 PATENT

66. **Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Second Amended Complaint as if fully set forth herein.**

67. **To the extent the preamble is limiting, each of the accused DDR4 LRDIMMs comprise a memory module operable to communicate with a memory controller via a memory bus. As an example, Samsung's website markets and contains datasheets for the accused DDR4 LRDIMMs:**



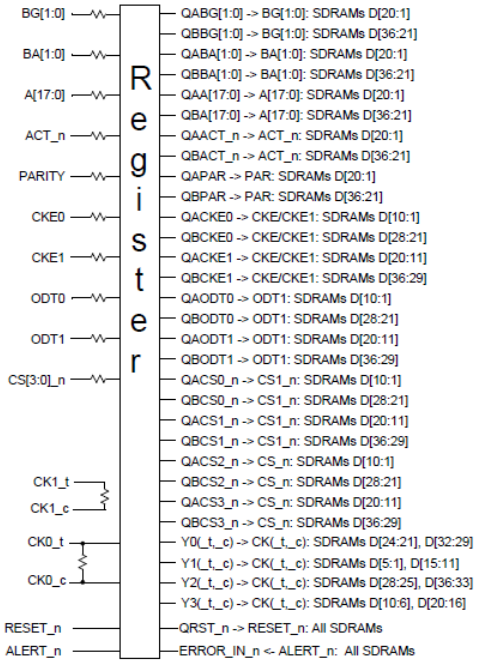
LRDIMM

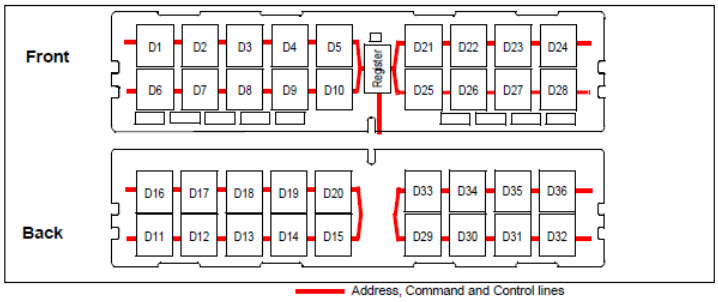
Load Reduced DIMM

- Include a register for enhancing clock, command and control signals
- Enhanced data signal by placing data buffer
- Best solution for achieving high density with high speed
- Supports x4 Organization / up to 4 ranks per DIMM and 3DPC
- Application : Server

(Depiction of an exemplary Samsung DDR4 LRDIMM advertised on its website, *available at* https://semiconductor.samsung.com/dram/module/lrdimm/m386a8k40bm1-crc/ (last accessed August 13, 2022)).

68. The memory bus of each accused LRDIMMs has signal lines that include a set of control/address signal lines and a plurality of sets of data/strobe signal lines.





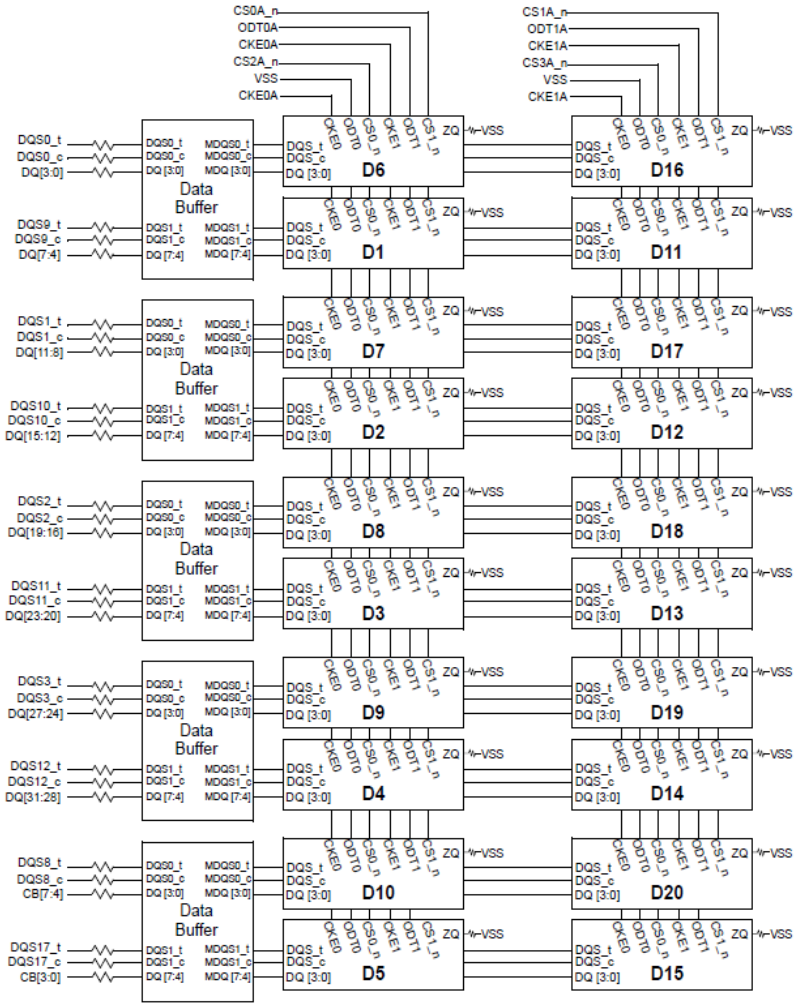
Ex. 6 at 10 (datasheet for M386A8K40BM1-CRC) (showing control/address signal lines).

5. Pin Description

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I2C serial bus clock for SPD/TS and register
BA0, BA1	Register bank select input	SDA	I2C serial bus data line for SPD/TS and register
BG0, BG1	Register bank group select input	SA0–SA2	I2C slave address select for SPD/TS and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	VPP	SDRAM activating power supply
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	Register clock enable lines input	VSS	Power supply return (ground)
ODT0, ODT1	Register on-die termination control lines input	VDDSPD	Serial SPD/TS positive power supply
ACT_n	Register input for activate input	ALERT_n	Register ALERT_n output
DQ0–DQ63	DIMM memory data bus	RESET_n	Set Register and SDRAMs to a Known State
CB0–CB7	DIMM ECC check bits	EVENT_n	SPD signals a thermal event has occurred
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)	VTT	SDRAM I/O termination supply
DQS0_c–DQS17_c	Data Buffer data strobes (negative line of differential pair)	RFU	Reserved for future use
CK0_t, CK1_t	Register clock input (positive line of differential pair)		
CK0_c, CK1_c	Register clocks input (negative line of differential pair)		

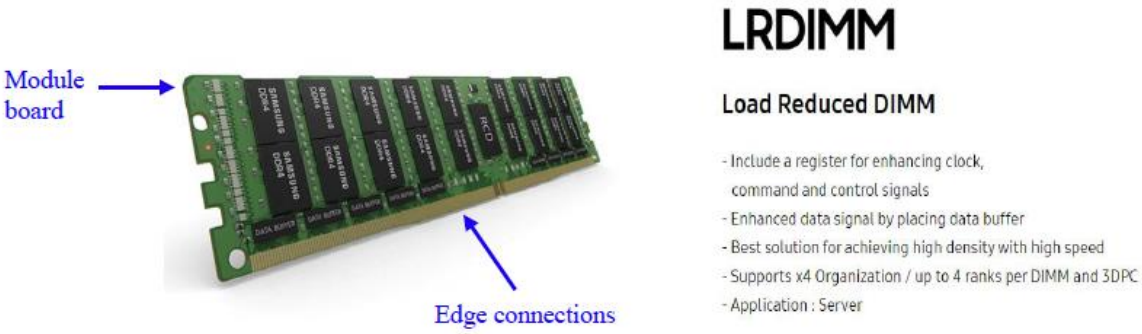
NOTE :
1. Address A17 is only valid for 16 Gb x4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

***Id.* at 6.**



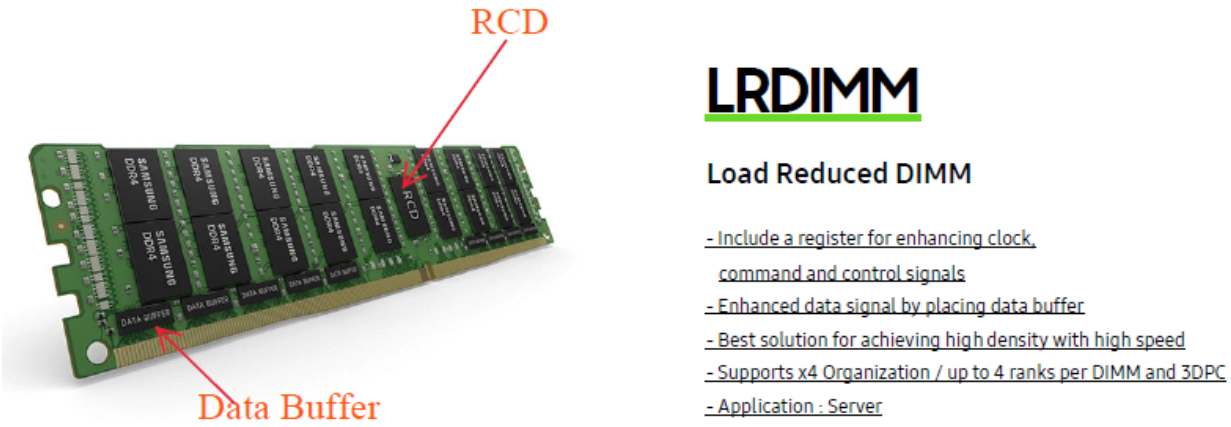
***Id.* at 11 (datasheet for M386A8K40BM1-CRC (showing the data/strobe signal lines)).**

69. The accused DDR4 LRDIMMs further each comprise a module board having edge connections to be coupled to respective signal lines in the memory bus, as illustrated in the examples below.



(Annotated depiction of an exemplary Samsung DDR4 LRDIMM advertised on its website, *available at* https://semiconductor.samsung.com/dram/module/lrdimm/m386a8k40bm1-crc/ (last accessed August 13, 2022)); *see also* Ex. 6 at 42 (datasheet for M386A8K40BM1-CRC).

70. The accused DDR4 LRDIMMs further each comprise a module control device (*e.g.*, a registering clock driver, or "RCD") on the module board configurable to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals. The module control device in each accused DDR4 LRDIMM is also configured to receive a system clock signal and output a module clock signal (*e.g.*, BCK_t/c). For example,

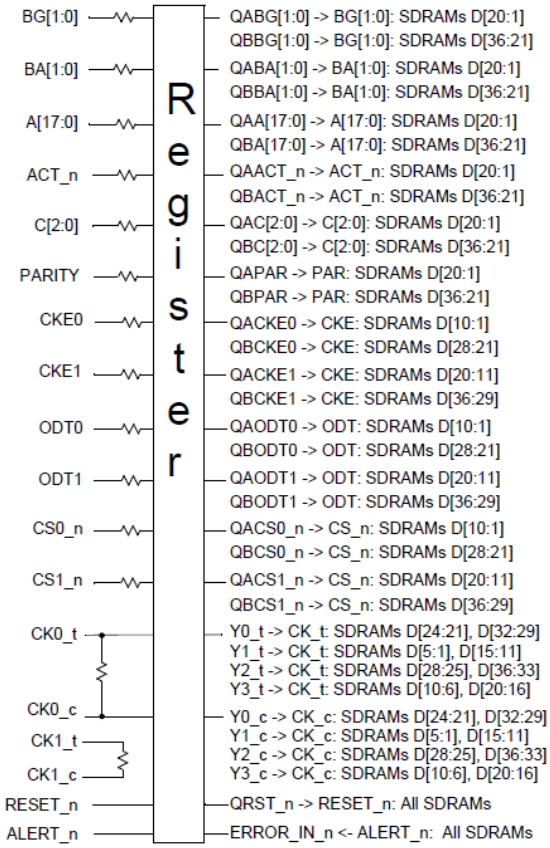


(Annotated depiction of an exemplary Samsung DDR4 LRDIMM advertised on its website, *available at* https://semiconductor.samsung.com/dram/module/lrdimm/m386a8k40bm1-crc/ (last accessed August 13, 2022)).

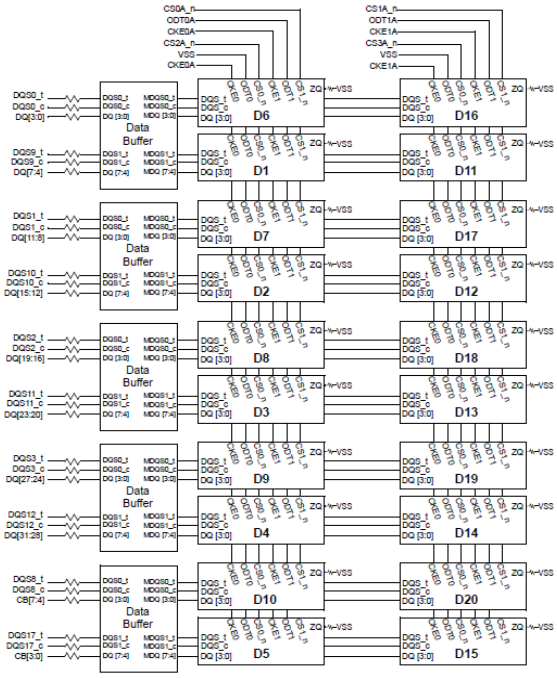
7. Input/Output Functional Description

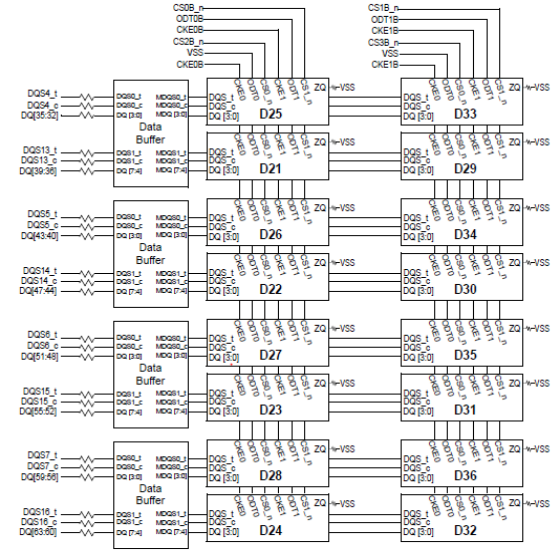
Symbol	Type	Function
CK0_t, CK0_c CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE, are disabled during power-down. Input buffers,excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0, C1	Input	Chip ID : Chip ID is only used for 3DS for 2and4 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/, signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. For x8 device, the function of DM is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifing whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH.
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. For x4/x8 based SDRAMs, BG0 and BG1 are valid. For x16 based SDRAM components only BG0 is valid.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A16	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR4 SDRAMs support differential data strobe only and does not support single-ended.

Ex. 6 at 7 (datasheet for M386A8K40BM1-CRC).



Id. **at 10 (datasheet for M386A8K40BM1-CRC).**

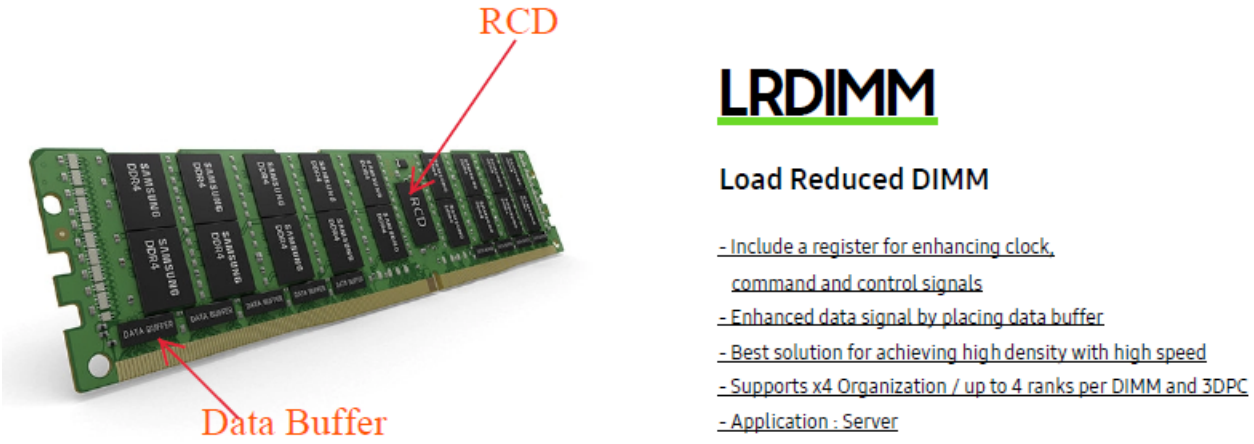




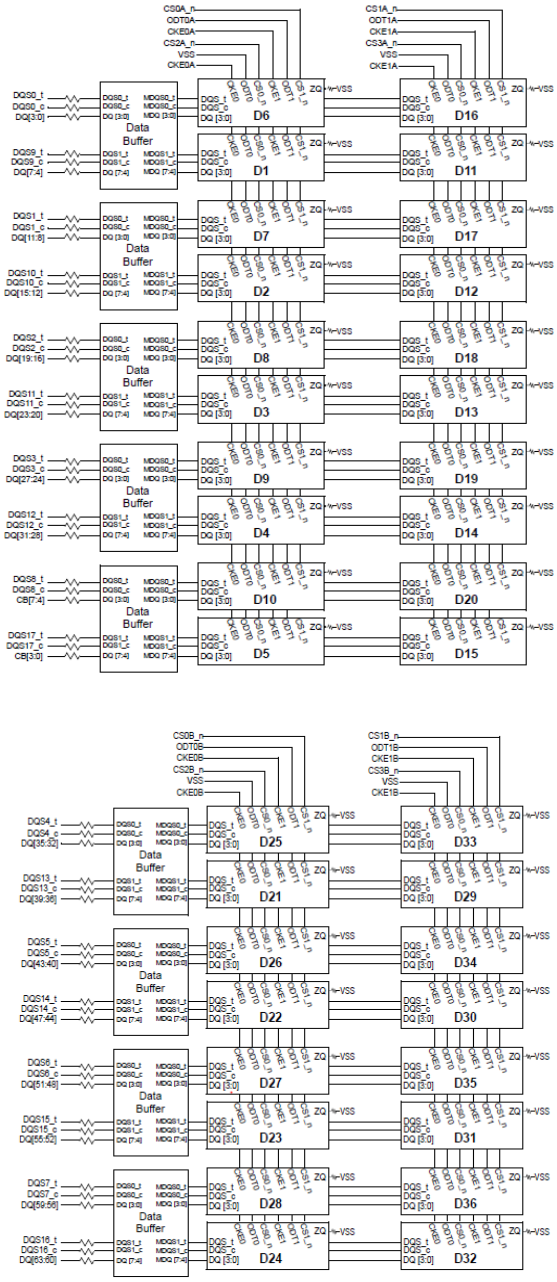
Id. **at 11-12. The JEDEC Standard No. 82-32A further discloses the module clock signals as BCK_t/BCK_c. *See* Ex. 7 at 2 (JEDEC Standard No. 82-32A (August 2019)) ("The clock inputs BCK_t and BCK_c are used to sample the control inputs**

BCOM[3:0], BCKE and BODT. The BCOM[3:0] inputs are used to write device internal control registers.").

71. Each of the accused DDR4 LRDIMMs includes memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals. The memory devices include a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines. For example, the accused DDR4 LRDIMM includes:



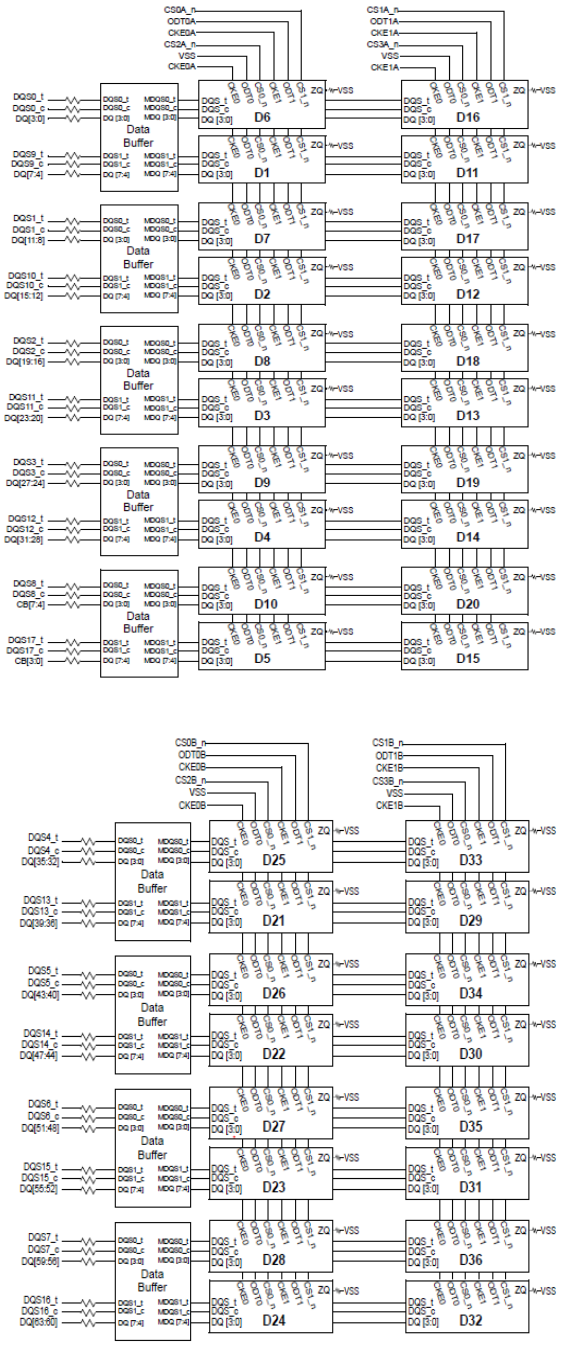
(Annotated depiction of an exemplary Samsung DDR4 LRDIMM advertised on its website, *available at* https://semiconductor.samsung.com/dram/module/lrdimm/m386a8k40bm1-crc/ (last accessed August 13, 2022)).



Ex. 6 at 11-12 (datasheet for M386A8K40BM1-CRC).

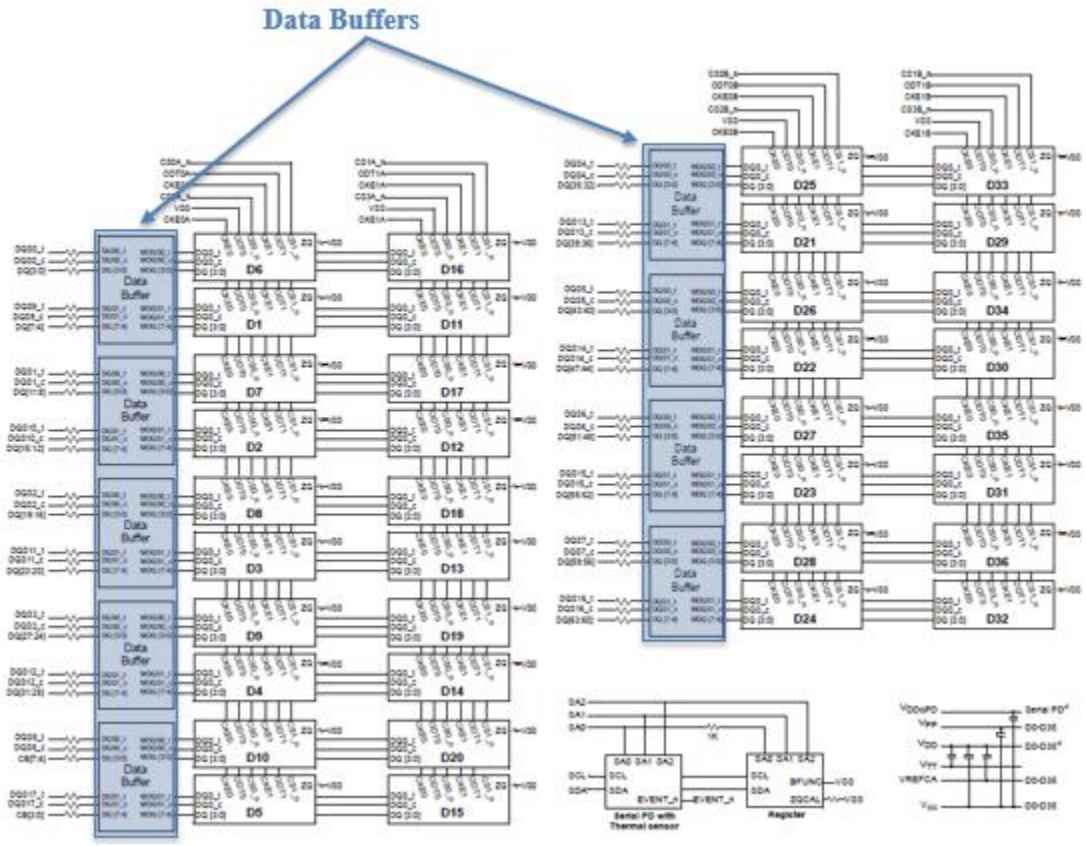
72. Each of the accused DDR4 LRDIMMs includes a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is

mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal. For example:

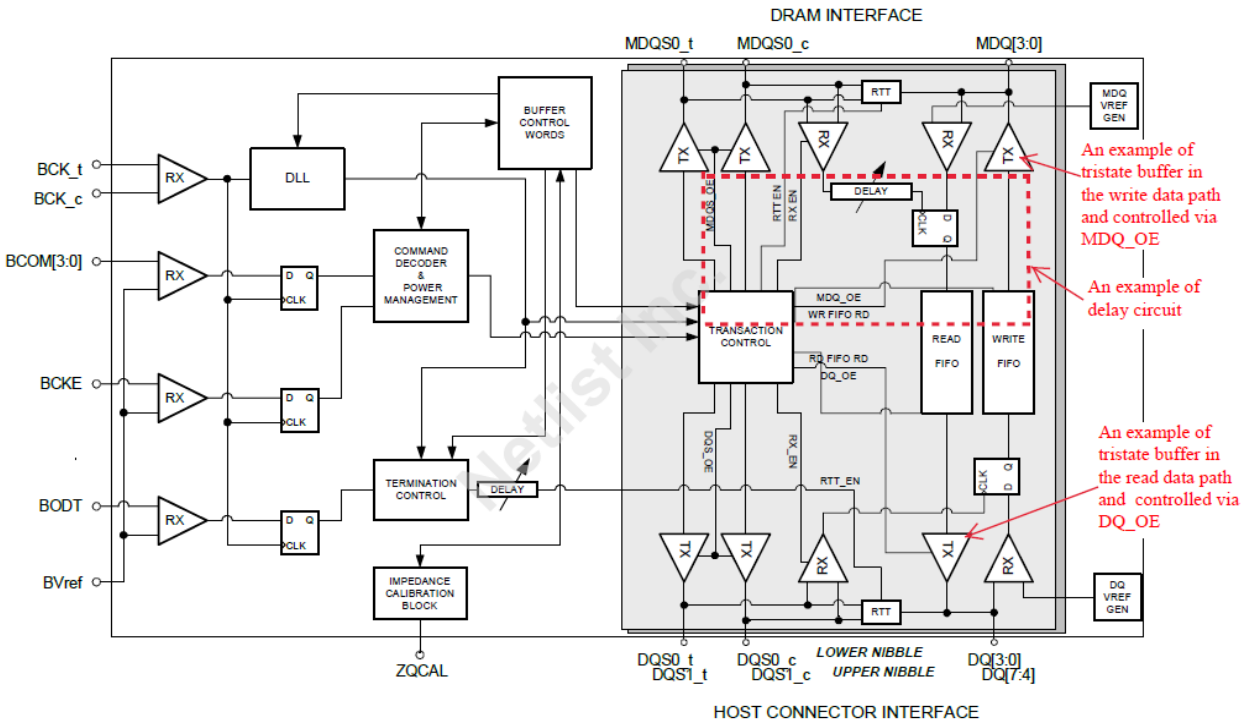


Id. **at 11-12 (datasheet for M386A8K40BM1-CRC).**

73. Each respective buffer circuit in the accused DDR4 LRDIMMs includes a data path corresponding to each data signal line in the respective set of data/strobe signal lines. Further, each respective buffer circuit in the accused DDR4 LRDIMMs includes a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal. For example:

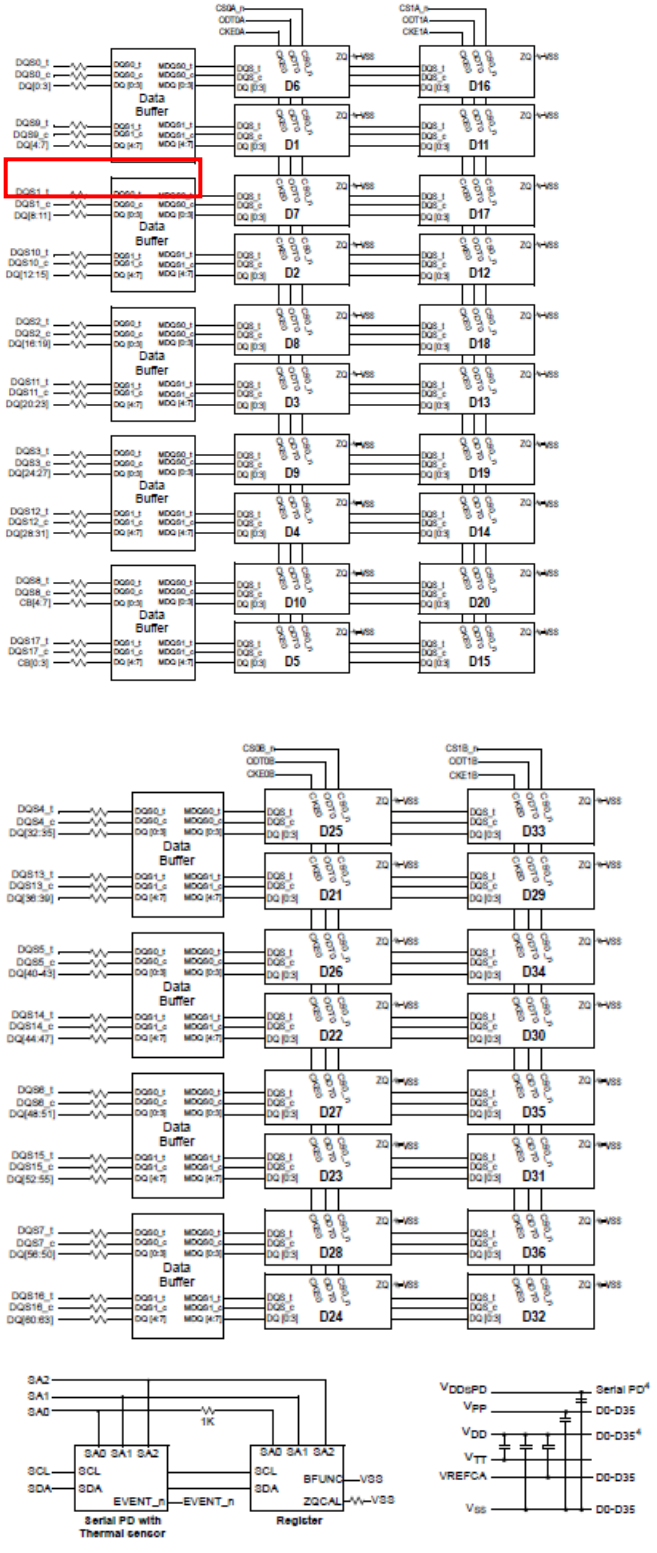


Id. **at 11-12 (datasheet for M386A8K40BM1-CRC).**



Ex. 7 (JEDEC Standard No. 82-32A (August 2019), Page 95).

74. As shown above in the example block diagram of Fig. 15 at page 95 of JEDEC Standard No. 82-32A, the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit. As shown above and below, the data path corresponding to the each data signal line also includes a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.



Ex. 6 (Datasheet for M386A8K40BM1-CRC) at 11-12.

75. Timing delays to be applied to data and data strobe signals are determined as described in at least section 2.12 starting at page 12 and in Table 16 at page 27 of JEDEC Standard No. 82-32A.

2.12 Command Sequence Descriptions

To accommodate the worst case DRAM CAS Latency, Additive Latency and Parity Latency, a DB is required to support a queue depth of 12 commands on the BCOM bus for data rates up to 2400MT/s.

The timing diagrams in this section show only the lower nibble of the DDR4DB02. The same timing relationships apply independently also for the upper nibble. The timing diagrams only show the case of burst length = 8 and preamble = 1 nCK but equivalent timing relationships exist for burst length = 4 & 10 and preamble = 2 nCK.

For readability reasons, the timing diagrams use the abbreviations DB_RL and DB_WL for the latency between first cycle of RD command and the first rising edge of MDQS at DDR4DB02 inputs and for the latency between first cycle of WR command and the first rising edge of MDQS at DDR4DB02 outputs respectively. Both DB_RL and DB_WL include full cycle and fractional cycle delays. The equations for these latencies are as follows:

$DB\_WL(R)^1 = CWL + AL + PL + DWL(R)$

$DB\_RL(R)^2 = CL + AL + PL + MRE(R) + tRPRE/2$

The equations for DWL and MRE for Ranks 0 to 3 are listed below.

where xxx[R].l and xxx[R].u are the equations for the lower and upper nibbles respectively

DWL[0].l = (F0BCDx[2:0] * 64 + F0BCAx[5:0]) * tCK/64

DWL[0].u = (F0BCDx[6:4] * 64 + F0BCBx[5:0]) * tCK/64

DWL[1].l = (F1BCDx[2:0] * 64 + F1BCAx[5:0]) * tCK/64

DWL[1].u = (F1BCDx[6:4] * 64 + F1BCBx[5:0]) * tCK/64

DWL[2].l = (F0BCFx[2:0] * 64 + F2BCAx[5:0]) * tCK/64

DWL[2].u = (F0BCFx[6:4] * 64 + F2BCBx[5:0]) * tCK/64

DWL[3].l = (F1BCFx[2:0] * 64 + F3BCAx[5:0]) * tCK/64

DWL[3].u = (F1BCFx[6:4] * 64 + F3BCBx[5:0]) * tCK/64

MRE[0].l = (F0BCCx[2:0] * 64 + F0BC2x[5:0]) * tCK/64

MRE[0].u = (F0BCCx[6:4] * 64 + F0BC3x[5:0]) * tCK/64

MRE[1].l = (F1BCCx[2:0] * 64 + F1BC2x[5:0]) * tCK/64

MRE[1].u = (F1BCCx[6:4] * 64 + F1BC3x[5:0]) * tCK/64

MRE[2].l = (F0BCEx[2:0] * 64 + F2BC2x[5:0]) * tCK/64

1.This equation assumes that the DDR4DB02 MDQ-MDQS Write Delay Control Words in F[3:0]BC8x/ F[3:0]BC9x are at their default power-on setting.

2.This equation assumes that the DDR4DB02 MDQS Read Delay Control Words in F[3:0]BC4x/F[3:0]BC5x are at their default power-on setting.

MRE[2].u = (F0BCEx[6:4] * 64 + F2BC3x[5:0]) * tCK/64

MRE[2].l = (F1BCEx[2:0] * 64 + F3BC2x[5:0]) * tCK/64

MRE[2].u = (F1BCEx[6:4] * 64 + F3BC3x[5:0]) * tCK/64

tRPRE/2 exists in DB_RL since the host will adjust the receive enable delay MRE(R) to place it in the center of the read preamble.

The DDR4DB02 delays tPDM_RD and tPDM_WR are defined as the delay between first rising edge of MDQS and the first rising edge of DQS for a RD command and as the delay between first rising edge of DQS and the first rising edge of MDQS for a WR command respectively. By default these delays are constant per DDR4DB02 for all ranks and nibbles.

***See* Ex. 7] at 11-12 (JEDEC Standard No. 82-32A (August 2019)). Each buffer circuit determines the rank ID of the specific set of memory devices, to be read from or to be written into, by decoding the module control signals, BCOM[3:0], during the second clock cycle after a properly received and decoded read or write commands during the first clock cycle.**

Table 4 — Multicycle Sequence for Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	WR	Write command BCOM[3:0] = 1000
2	DAT0	Transfer the rank ID for write command BCOM[1:0] = {RANK_ID[1:0]} for DRAM writes Burst length information for Write data BCOM[3:2] = {0, 0} for BC4 BCOM[3:2] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for WR command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

***See Id.* at 12 (JEDEC Standard No. 82-32A (August 2019)).**

Table 5 — Multi-cycle Sequence for Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	RD	Read command BCOM[3:0] = 1001
2	DAT0	Transfer the rank ID for read command or the MPR selection ID in MPR override read mode BCOM[1:0] = {RANK_ID[1:0]} for DRAM reads BCOM[1:0] = {BA1, BA0} for MPR override reads Burst length information for Read data BCOM[3:0] = {0, 0} for BC4[1] BCOM[3:0] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for RD command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

See Id. **at 14 (JEDEC Standard No. 82-32A, (August 2019)).**

Table 16 — Timing and Training Control Words

Address	Description	Scope
BC0C	Training control word	Training mode enable
F0BCCx	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 0	Additional cycles of DRAM Interface Receive Enable Delay and Write Leveling Delay per rank and per nibble
F0BCDx	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 0	
F0BCEx	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 2	
F0BCFx	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 2	
F1BCCx	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 1	
F1BCDx	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 1	
F1BCEx	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 3	
F1BCFx	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 3	
F[3:0]BC2x	Lower nibble DRAM interface receive enable training control	DRAM Interface Receive Enable phase and cycle control per rank
F[3:0]BC3x	Upper nibble DRAM interface receive enable training control	
F[3:0]BC4x	Lower nibble MDQS read delay control	Input MDQS delay control per rank
F[3:0]BC5x	Upper nibble MDQS read delay control	
F[3:0]BC8x	Lower nibble MDQ-MDQS write delay control	Output MDQ signal phase control per rank
F[3:0]BC9x	Upper nibble MDQ-MDQS write delay control	
F[3:0]BCAx	Lower nibble host interface write leveling control	Host Interface write leveling phase and cycle control per rank
F[3:0]BCBx	Upper nibble host interface write leveling training control	
F5BC0x - F5BC3x F6BC0x - F6BC3x	Lower and upper nibble Multi Purpose Registers[7:0]	Store read/write data patterns for receive enable, read and write delay and host interface write training as well as MPR override mode.
F6BC4x	Buffer training configuration control word	Configuration control for certain training modes
F6BC5x	Buffer training status word	Status for certain training modes
F[7:4]BC8x	MDQ0/4-Read delay control	Input MDQS delay control per rank and per lane
F[7:4]BC9x	MDQ1/5-Read delay control	
F[7:4]BCAx	MDQ2/6-Read delay control	
F[7:4]BCBx	MDQ3/7-Read delay control	
F[7:4]BCCx	MDQ0/4-MDQS write delay control	Output MDQ signal phase control per rank and per lane
F[7:4]BCDx	MDQ1/5-MDQS write delay control	
F[7:4]BCEx	MDQ2/6-MDQS write delay control	
F[7:4]BCFx	MDQ3/7-MDQS write delay control	

See Id. **at 27 (JEDEC Standard No. 82-32A (August 2019)) (demonstrating timing control registers and fields corresponding to timing delays information per rank and/or per lower or upper nibble of each buffer circuit).**

76. On information and belief, Samsung also indirectly infringes the '608 patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as

Samsung's customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has induced, and currently induces, the infringement of the '608 patent through its affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the accused DDR4 LRDIMM products and other materially similar products that infringe the '608 patent. On information and belief, Samsung provides, and has provided, specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing use of the accused DDR4 LRDIMM products and other materially similar products by users in a manner that it knows or should have known would result in infringement and with the intent of inducing infringement.

77. On information and belief, Samsung also indirectly infringes the '608 patent, as provided in 35 U.S.C. § 271(c), by contributing to direct infringement committed by others, such as customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Samsung has contributed to, and currently contributes to, Samsung's customers' and end-users' infringement of the '608 patent through its affirmative acts of selling and offering to sell, in this District and elsewhere in the United States, the accused DDR4 LRDIMM products and other materially similar products that infringe the '608 patent. On information and belief, the accused DDR4 LRDIMM and other materially similar products have no substantial noninfringing use, and constitute a material part of the patented invention. On information and belief, Samsung is aware that the product or process that includes the accused DDR4 LRDIMM products and other materially

similar products would be covered by one or more claims of the '608 patent. On information and belief, the use of the product or process that includes the accused DDR4 LRDIMM products infringes at least one claim of the '608 patent.

78. Samsung's infringement of the '608 patent has damaged and will continue to damage Netlist. Samsung has had actual notice of the application that issued as the '608 patent since at least August 2, 2021. Samsung's infringement of the '608 patent has been continuing and willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its actions constituted an unjustifiably high risk of infringement.

VIII. ~~§II.~~DEMAND FOR JURY TRIAL

79. ~~64.~~Pursuant to Federal Rule of Civil Procedure 38(b), Netlist hereby demands a trial by jury on all issues triable to a jury.

IX. ~~§III.~~PRAYER FOR RELIEF

WHEREFORE, Netlist respectfully requests that this Court enter judgment in its favor ordering, finding, declaring, and/or awarding Netlist relief as follows:

A. that Samsung infringes the Patent-in-Suit;

B. all equitable relief the Court deems just and proper as a result of Samsung's infringement;

C. an award of damages resulting from Samsung's acts of infringement in accordance with 35 U.S.C. § 284;

D. that Samsung's infringement of the Patents-in-Suit is willful;

E. enhanced damages pursuant to 35 U.S.C. § 284;

F. that this is an exceptional case and awarding Netlist its reasonable attorneys' fees pursuant to 35 U.S.C. § 285;

G. an accounting for acts of infringement and supplemental damages, without limitation, prejudgment and post-judgment interest; and

H. such other equitable relief which may be requested and to which Netlist is entitled.

Dated: ~~August 15, 2022~~**January 20, 2023**

Respectfully submitted,

/s/ Jason Sheasby

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